10.4 A Wheatstone Bridge Temperature Sensor with a Resolution FoM of 20fJ·K²

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Temperature sensors intended for embedded applications should be both energy- and area-efficient. The combination of Wheatstone-bridge (WhB) sensors and continuous-time ADCs has proven to be highly energy efficient [1,2]. However, their area (> 0.25mm²) is still larger than that of comparable BJT-based sensors [3,4]. This paper presents a temperature sensor that uses an FIR-DAC ADC to reduce its area and increase energy-efficiency, both by 2× compared to the state-of-the-art [5].

A simplified model of the sensor is shown in Fig. 10.4.1 (top). To maximize its sensitivity, the WhB consists of resistors R_p (105kΩ, silicided p-poly) and R_n (100kΩ, non-silicided n-poly) with positive and negative temperature coefficients (TCs), respectively [1,2]. Its temperature-dependent output current I_{sig} is then digitized by a continuous-time delta-sigma modulator (CTΔΣM), which balances I_{sig} with the current I_{DAC} generated by a 2b resistive DAC R_{DAC} (4×720kΩ, non-silicided n-poly).

The use of a multi-bit DAC reduces the swing of the loop filter input current I_{err}, which decreases the power dissipation of the 1st integrator and the area of C_{int}. In [2], a zoom ADC is used, and the DAC state is determined by combining the result of an initial coarse SAR conversion with the output of a 1b CTΔΣM. Extra logic is then required to implement the SAR conversion, as well as the data-weighted-averaging (DWA) and segment-averaging schemes used to mitigate DAC mismatch and amplifier non-linearity, respectively.

In this design, a 1b CTΔΣM drives a FIR-DAC, thus ensuring 1b linearity without the need for extra logic [6]. For the same DAC resolution, the resulting I_{err} swing will then be about 2× less than that in the zoom ADC of [2], since the FIR-DAC does not require over-ranging (Fig. 10.4.1, bottom). As a result, both the size and area of C_{int} can be reduced, as well as the power dissipation of the 1st integrator .

Due to the uncorrelated spread of R_p and R_n, the nominal range of the WhB output current I_{sig} will spread significantly from batch to batch. To compensate for this, and so make optimal use of the input dynamic range of the modulator, a 4b batch trim is applied to R_p (~5.7kΩ/step). As shown in Fig. 10.4.2, the trimming scheme ensures that only one switch is in series with the selected segment of R_p. Compared to the trimming scheme in [1], this minimizes temperature-sensing errors due to the switches' finite on-resistance.

To achieve sub-mK resolution in a short conversion time (t_{conv} = 10ms), the modulator employs a 2nd-order feedforward architecture (Fig. 10.4.2). This also reduces the swing at the output of the 1st integrator, and thus reduces the area of C_{int1}. The 2nd stage consists of a switched-capacitor integrator (C_{S2} and C_{int2}) and a feedforward path (C_{FF2}). An extra FIR filter ($C_{FIR,C}$), is used to compensate for the delay introduced by the FIR-DAC [6].

As shown in Fig. 10.4.3, the opamp used in the 1st integrator consists of two current-reuse stages. This maximizes the noise efficiency of the input stage, and, compared to the use of two common-source amplifiers, halves the output stage bias current for a given maximum output current. The output stage uses high threshold devices to achieve a large output swing (~1.5V at room temperature (RT)). This, in turn, allows the area of C_{int1} to be further reduced. Compared to the OTA used in [2], which has a closed-loop input impedance of 1/gm, the closed-loop input impedance of the opamp is much lower, reducing its input swing and thus improving its linearity. The input stage is chopped to suppress its offset and 1/*f* noise, and so the chopping frequency f_{chop} must be chosen such that quantization noise is not downconverted to DC. In this design, f_{chop} can be set to either f_s = 500kHz [2] or, by exploiting the spectral notches of the FIR-DAC, to f_s/8 [6]. From simulations, the chopped opamp has a residual 1/*f* corner frequency of 2Hz, and a DC gain of 80dB, while its input/output stages consume 15μW/11μW, respectively. The 2nd stage is built around a cascoded telescopic OTA, which also has 80dB gain, but consumes only 3.5μW.

Two identical sensors were fabricated on the same die in a 0.18μm CMOS process (Fig. 10.4.7). This allows their resolution to be accurately estimated via differential measurements, which effectively reject ambient temperature drift. Each sensor consumes about 44μA (41μA analog and 3μA digital) from a 1.8V supply, and occupies 0.12mm², 60% of which is occupied by the WhB and the DAC. The sensors share the same clock generation circuit (0.003mm²). To further conserve area, C_{int1} (27pF, MIM) is located directly above the WhB. For flexibility, the sinc² decimation filters are implemented off-chip.

20 samples from one wafer (40 sensors) were mounted in ceramic DIL packages and characterized in a temperature-controlled oven. The packages were mounted in good thermal contact with a large aluminum block. After a batch trim, the residual spread from sample to sample is less than ± 3% full scale at RT. To mimic the effect of batch-to-batch spread, the sensor's output was characterized over temperature for two different trim code settings (Fig. 10.4.4 (top left)). After a 1st-order fit to compensate for process spread [2], the resulting systematic non-linearity differs by less than 3mK for the two trim-code settings, it also agrees well with simulations (less than 0.1°C difference) and so can be robustly corrected by a fixed 5th-order polynomial. The sensor then achieves an inaccuracy of 0.14°C (3σ) from –55°C to 125°C for both trim code settings (Fig. 10.4.4 (bottom)). Its supply sensitivity is quite low: ~0.03°C/V from 1.6 to 2V at RT. This remains constant up to about 500Hz, above which it exhibits a first-order roll-off due to the finite bandwidth of the 1st integrator's opamp.

FFTs of the sensor's bitstream output are shown in Fig. 10.4.5 (top). As designed, the sensor's noise is dominated by the WhB, and so changing f_{chop} from f_s to f_s/8 has no significant effect on its resolution. The observed 1/*f* noise (~20Hz corner frequency) is mainly due to the non-silicided poly resistors of the WhB [2]. Computing the standard deviation from the output of a single sensor over a long (20s) interval results in an estimated resolution that mainly reflects oven drift (Fig. 10.4.5 (bottom)). The effect of oven drift can be suppressed by computing the standard deviation from the difference in the output of the two sensors on each die. Alternatively, a shorter measurement interval can be used. As shown in Fig. 10.4.5 (bottom), over a 1s interval, the results of the single-ended and differential approaches agree well, resulting in a resolution of 160μK (rms) for t_{conv} = 10ms. With the differential approach, the effect of the sensor's own 1/*f* noise can be clearly seen: the resolution gets worse for longer (20s) measurement intervals.

In Fig. 10.4.6, the performance of this FIR-DAC WhB sensor is summarized and compared with state-of-the-art. It achieves the best FoM, improving on the state-of-the-art [2] by 2×. It is also the most compact high-resolution (sub-mK) temperature sensor, and is smaller than most precision BJT sensors [3,4]. These features make the sensor well suited for embedded applications in which both high-resolution and accuracy are required.

Acknowledgment:
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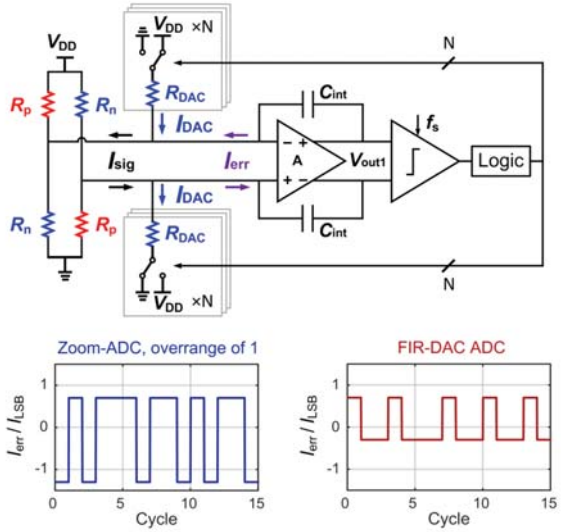

Figure 10.4.1: CTΔΣ readout of a differential Wheatstone bridge temperature sensor (top), error current I_{err} over time (bottom).

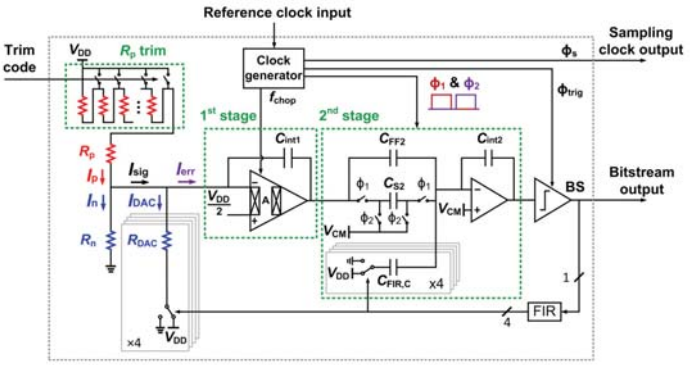

Figure 10.4.2: Simplified single-ended system block diagram.

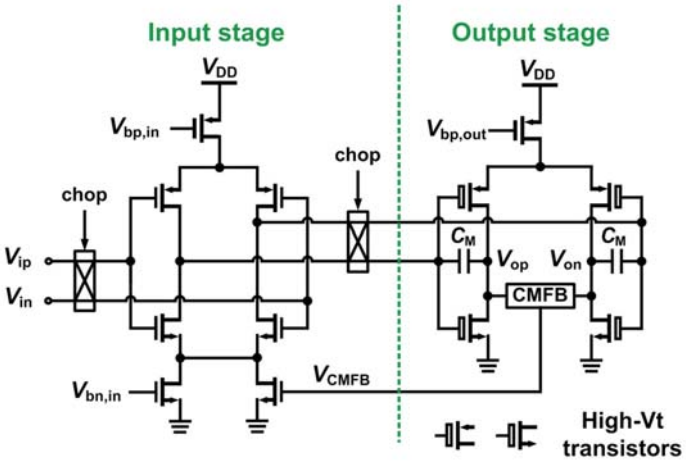

Figure 10.4.3: Schematic diagram of the 1st-stage opamp.

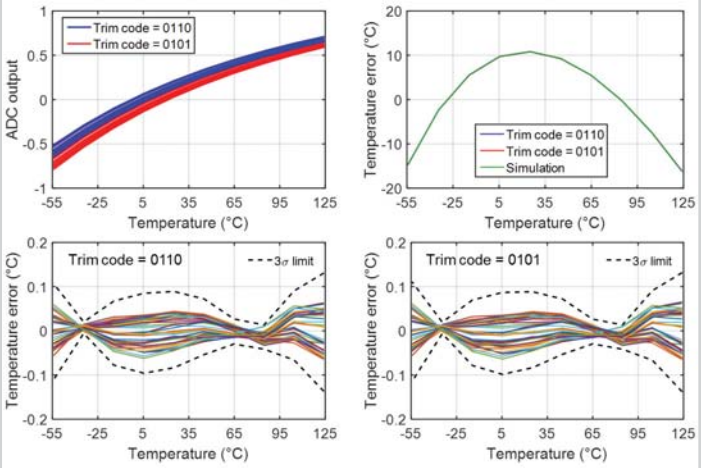

Figure 10.4.4: The sensor's characteristic (top left), systematic nonlinearity after a 1st-order fit (top right) and temperature error after individual 1st-order fit and fixed nonlinearity removal (bottom).

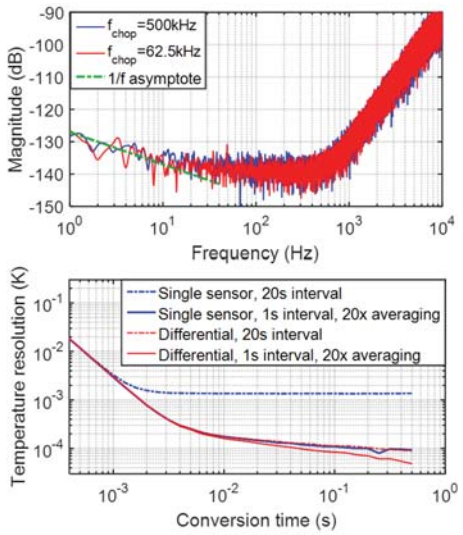

Figure 10.4.5: PSD of the sensor's bitstream (top), resolution vs. time plot (bottom).

	[7]	[3]	[4]	[1]	[2]	This work
Sensor type	Dual-MEMS Resonator	BJT	BJT	Resistor WhB	Resistor WhB	**Resistor WhB**
CMOS Technology	0.18µm	0.16µm	0.18µm	0.18µm	0.18µm	**0.18µm**
Area [mm²]	0.54	0.16	0.198	0.43	0.25	**0.12**
Temperature range	-40°C to 85°C	-70°C to 125°C	25°C to 45°C	-45°C to 125°C	-55°C to 125°C	**-55°C to 125°C**
3σ inaccuracy [°C] (Trimming points)	--	0.06 (1)	0.2 (1)	0.4 (2 [a])	0.12 (2 [b])	**~0.14 (2 [b])**
Supply voltage [V]	1.6	1.6	1 (analog) 1.8 (digital)	1.5	1.8	**1.8**
Power consumption [µW]	13000	7	1.1	65	94	**79**
Conversion time [ms]	5	5	500	0.1	5	**10**
Resolution [mK]	0.02	15	10	10	0.29	**0.16**
Resolution FoM [fJ·K²] [c]	40	7300	55000	650	40	**20**

[a] 1 point trim + 1st order fit. [b] 1st order fit. [c] FoM = Energy / Conversion x (Resolution)².

Figure 10.4.6: Performance summary and comparison with previous work.

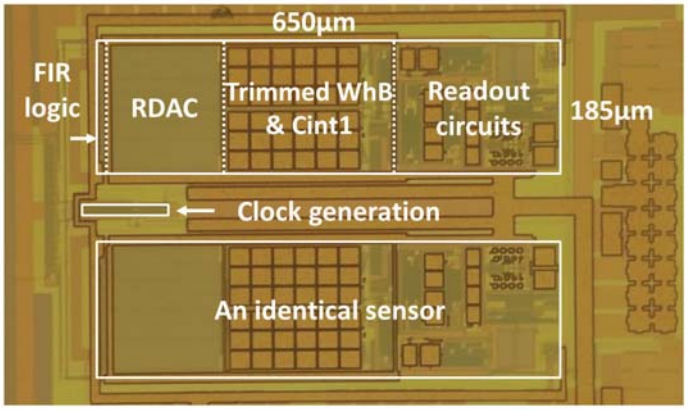

Figure 10.4.7: Die micrograph of the fabricated temperature sensor.

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