5.3 A Highly Digital 2210μm² Resistor-Based Temperature Sensor with a 1-Point Trimmed Inaccuracy of ±1.3°C (3σ) from -55°C to 125°C in 65nm CMOS

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Microprocessors and SoCs employ multiple temperature sensors to prevent overheating and ensure reliable operation. Such sensors should be small (<10,000μm²) to monitor local hot-spots in dense layouts. They should also be moderately accurate (~1°C) up to high temperatures (≥125°C), so that the system throttling temperature can be set as close as possible to the maximum allowable die temperature. Furthermore, they should be fast (~1kS/s) and consume low power (tens of μW).

Compact resistor-based temperature sensors can meet most of these requirements. As shown in Fig. 5.3.1 (left), they often consist of a frequency-locked loop (FLL), which maintains a constant phase shift (ϕ_{ref}) in an RC filter by adjusting its drive frequency (F_{drive}) in a temperature-dependent manner [1,2]. Mainly due to their use of analog loop filters, however, they typically occupy more than 5,000μm², and are difficult to scale. Alternatively, an RC filter can be driven at a constant frequency and the resulting temperature-dependent phase-shift can then be digitized by a highly digital phase-domain delta-sigma modulator (PDΔΣM), as shown in Fig. 5.3.1 (right) [3]. A current-controlled oscillator (CCO) converts the filter's output into a frequency-modulated square-wave that can be integrated by a counter. The modulator's phase summation node is then realized by using the output of its phase DAC to control the counter's up/down action. The sensor occupies 6800μm² in 0.18μm CMOS [3], and can be made much smaller in 40nm [4]. However, the CCO's non-linear current-to-frequency characteristic limits the sensor's inaccuracy to ±2.7°C (3σ) from -35°C to 125°C after a 1-point trim. Furthermore, the time-domain quantization noise (Q-noise) associated with the counter significantly degrades the sensor's resolution (120mK).

In this work, a resistor-based temperature sensor based on an improved highly digital PDΔΣM is presented. Its two key architectural innovations are 1) the use of dual gated-ring-oscillators (GROs) to shape the counter's time-domain Q-noise, and 2) their operation at a fixed frequency, which enables linear phase detection. Compared to previous PDΔΣM-based designs [3,4], the sensor achieves ~10× more resolution (12.8mK resolution in a 1ms conversion time), while consuming ~50× less power (28μW). Furthermore, compared to previous FLL-based designs [1,2], it achieves similar inaccuracy (±1.3°C (3σ), 1-pt trim), but over the full military temperature range (-55°C to 125°C). It also occupies ~3× less area (2210μm²) and is highly scalable.

The use of a counter to integrate CCO phase gives rise to time-domain Q-noise. This is illustrated in Fig. 5.3.2, in which the CCO's phase increases by 3.6 cycles during every counting cycle. Since the counter cannot accumulate fractional phase, time-domain Q-noise will be accumulated at the end of each cycle, thus limiting the resolution. This can be reduced by increasing the CCO's frequency swing, but this increases power consumption and non-linearity.

In this work, the single CCO and the up/down counter of [3,4] are replaced by dual GRO/counter pairs, one for counting "up" and the other for counting "down". Their outputs are then digitally subtracted to generate the final integrated result. This approach prevents the accumulation of time-domain Q-noise and results in 1st-order noise shaping. As shown in Fig. 5.3.2, the fractional phases of each oscillator can be preserved by disconnecting their supply currents, which disables their inverters but preserves their output states [5]. The resulting GROs can be operated at 50MHz, compared to the 800MHz in [3,4], drastically reducing the counters' power dissipation.

Figure 5.3.3 shows the schematic of the proposed resistor-based temperature sensor. It consists of a 2-bit 1st-order PDΔΣM that digitizes the phase-shift of a polyphase filter (PPF). When driven by a square-wave F_{drive}, the zero-crossings of the PPF's output exhibit a temperature-dependent phase-shift, which can readily be digitized by a comparator, similar to the one in [2]. To save area, the PPF's capacitors (MIM, 1pF) are located above its resistors (silicided polysilicon, 100kΩ). When F_{drive} = 2.25MHz, the phase of the comparator's square-wave output varies from about 80° to 120° over a temperature range from -55°C to 125°C. When operated at a sampling rate $F_s = F_{drive}$, a 2-bit phase DAC (φ_{DAC} = 67.5°, 90°, 112.5°, and 135°) ensures sufficiently low Q-noise (~4mK rms) in the targeted 1ms conversion time.

The PDΔΣM's phase summation node consists of an XOR gate, used as a linear phase detector. Its output enables either the "up" or the "down" GRO by connecting them to a constant current source I_{in} that is derived from a central biasing circuit. With the chosen phase DAC range and oscillation frequency, 7-bit counters are enough to prevent overflow at the end of each ΔΣ cycle [6]. To save power, the subtractor is only enabled (by FS_{en}) shortly before the rising edge of the sampling clock (FS). Compared to [3,4], this architecture has two main advantages: 1) it is highly linear, due to the use of a linear phase detector and the absence of CCOs in the analog signal path, and 2) it is highly scalable, because, apart from the PPF and the comparator, it mainly consists of synthesized digital logic.

However, GRO mismatch and drift lead to offset and drift in the digitized phase output. To suppress these, the GROs are chopped, by periodically swapping their positions with the help of an XOR-gate and two multiplexers. To minimize transient errors due to the stored GRO phase, this is only done once per conversion, i.e. at 1kHz (ChL). As shown in Fig. 5.3.3, a sinc² filter is used to decimate the PDΔΣM's output during each phase and the results are then averaged to compensate for the chopper ripple.

The prototype sensor is fabricated in a 65nm CMOS technology (Fig. 5.3.7). It occupies an area of 2210μm² and consumes 28μW (74% PPF + comparator, 16% GRO, and 10% digital) at room temperature from a 0.9V supply. The PDΔΣM's PSD is shown in Fig. 5.3.4 (top). It exhibits 1st-order noise shaping and shows that GRO drift is effectively suppressed by chopping. Figure 5.3.4 (bottom) shows the sensor's resolution versus conversion time. With chopping enabled, the sensor achieves a 12.8mK resolution in a 1ms conversion time. A total of 96 sensors from 4 chips were characterized. Over the military temperature-range, their output phase varies by about 33° (Fig. 5.3.5, top-left). The sensor's characteristic is quite linear and only exhibits a small systematic non-linearity (about 6°C) over the military temperature range (Fig. 5.3.5, bottom-left). Simulations show that this is mainly due to the resistor's non-linear TC (Fig. 5.3.5, bottom-right), and can be removed by a fixed 3rd-order polynomial. This results in an inaccuracy of ±1.3°C (3σ) over the military temperature range after a correlated 1-pt trim [7].

Figure 5.3.6 shows a performance summary and comparison to other state-of-the-art temperature sensors for thermal management. Compared to other resistor-based sensors [1-3], this work occupies ~3× less area and achieves comparable inaccuracy up to higher temperatures (125°C). Compared to BJT-based sensors, it achieves comparable area in a more mature process, but is much more scalable, since its supply voltage is not limited by V_{BE}, and most of its circuitry consists of synthesized digital logic.

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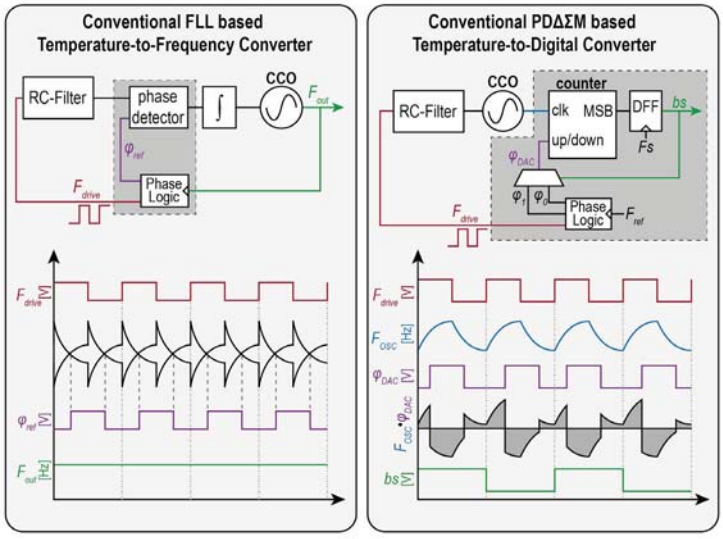

Figure 5.3.1: Simplified block diagram of FLL- and PDΔΣM-based temperature sensors.

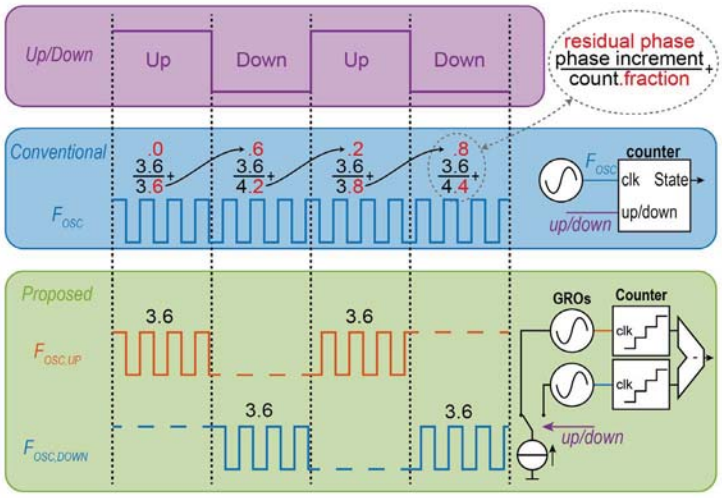

Figure 5.3.2: Time-domain Q-noise in VCO- and GRO-based Up/Down counters.

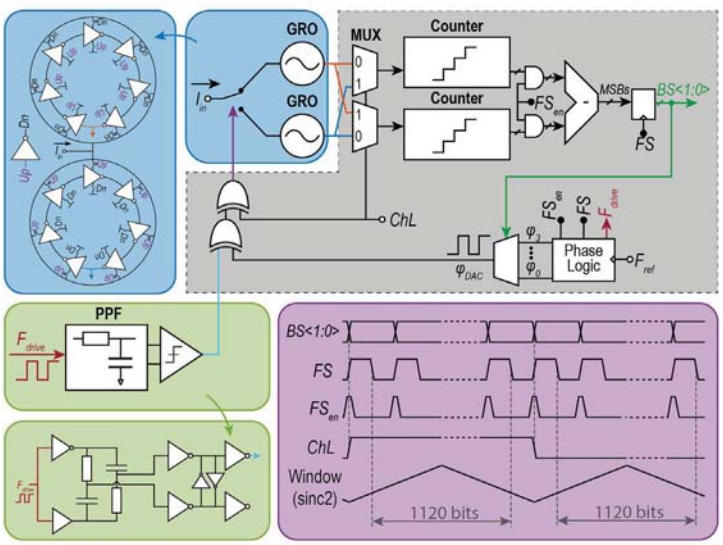

Figure 5.3.3: Complete system diagram and waveforms illustrating its operation.

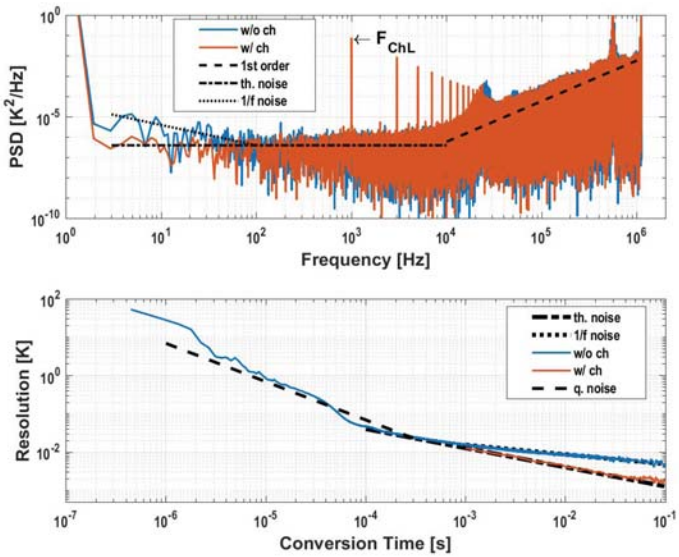

Figure 5.3.4: PSD of the sensor's bitstream (top, Hanning window, 1,048,576 samples) and its resolution vs. conversion-time (bottom).

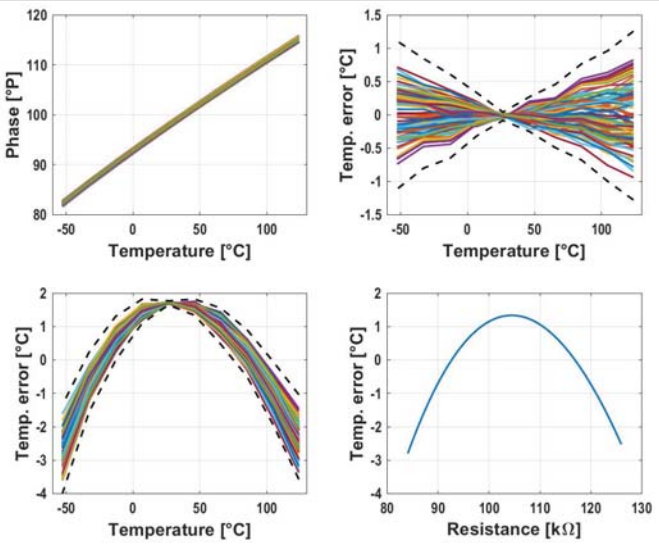

Figure 5.3.5: Sensor output phase (top-left); error after a correlated 1-pt trim + 3rd-order polynomial (top-right); error after a correlated 1-pt trim (bottom-left), and simulated non-linearity of the sensor (bottom-right).

	This work	ISSCC20 Khashaba [1]	SSCL19 Lee [2]	JSSC17 Sonmez [4]	SSCL19 Eberlein	ISSCC18 Lu
Sensor type	Resistor PDΔΣM	Resistor FLL	Resistor FLL	TD PDΔΣM	Diode SAR	BJT-MOS SAR
Process	65nm	65nm	65nm	40nm	16nm	22nm
Area [μm²]	**2 210**	8 800	5 800	1 650	2 500	4 300
Temperature Range [°C]	**-55 to 125**	-30 to 90	-50 to 105	-55 to 125	-15 to 105	-30 to 120
Accuracy [°C]	±1.3 (3σ)	±0.72 (p2p)	±1.2 (3σ)	±1.4 (3σ)	+1.5/-2.0 (p2p)	±1.07 (3σ)
Trimming	1-pt	1-pt	1-pt	0-pt	0-pt	1-pt
Power [μW]	**28**	45	32.5	2 500	18	50
Supply voltage [V]	0.9	1	1	1.05	0.95	1
Conversion time [ms]	1	1	1	1	0.013	0.032
Resolution [mK]	**12.8 (rms)**	1.43 (rms)	2.8 (rms)	360 (rms)	300 (lsb)	580 (lsb)
PSS [°C/V]	9.1	2.2	0.22	2.8	1.5	1.76

Figure 5.3.6: Performance summary and comparison with prior art.

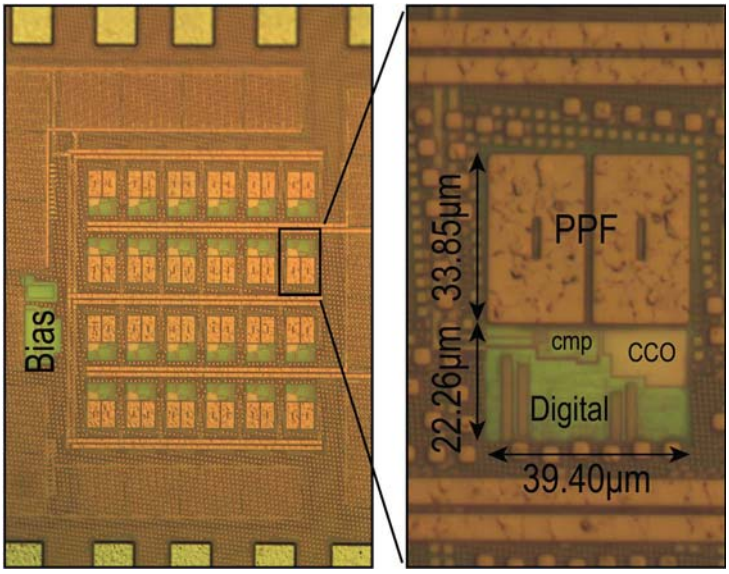

Figure 5.3.7: Die micrograph of the fabricated temperature sensor.

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