A PNP-Based Temperature Sensor With Continuous-Time Readout and ±0.1 °C (3σ) Inaccuracy From −55 °C to 125 °C

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***Abstract*— This article describes a PNP-based temperature sensor that achieves both high energy efficiency and accuracy. Two resistors convert the CTAT and PTAT voltages generated by a PNP-based front-end into two currents whose ratio is then digitized by a continuous-time (CT) ΔΣ-modulator. Chopping and dynamic-element-matching (DEM) are used to mitigate the effects of component mismatch and 1/f noise, while the spread in V_{BE} and in the ratio of the two resistors is digitally trimmed at room temperature (RT). Fabricated in a 0.18 μm CMOS process, the sensor occupies 0.12 mm^2, and draws 9.5 μA from a supply voltage ranging from 1.7 to 2.2 V. Measurements on 40 samples from one batch show that it achieves an inaccuracy of ±0.1 °C (3σ) from −55 °C to 125 °C, and a commensurate supply sensitivity of only 0.01 °C/V. Furthermore, it achieves high energy efficiency, with a resolution Figure of Merit (FoM) of 0.85 pJ·K^2.**

***Index Terms*— Bitstream-controlled (BSC) dynamic-element-matching (DEM), continuous-time (CT) ΔΣ-modulator, current-mode readout, PNP-based temperature sensor, resistor ratio self-calibration.**

I. Introduction

BJT-BASED temperature sensors are widely used since they can achieve high accuracy after a single temperature trim [1]. Readout architectures based on switched-capacitor (SC) ΔΣ-modulators [2], [3], [4], [5] can achieve inaccuracies below 0.2 °C (3σ) from −55 °C to 125 °C after a room temperature (RT) trim. However, their sampling (kT/C) noise reduces their resolution and energy efficiency. Readout architectures based on continuous-time (CT) ΔΣ-modulators do not suffer from sampling noise and thus achieve lower noise and better energy efficiency [6], [7]. However, they have not yet been able to match the accuracy of their SC counterparts.

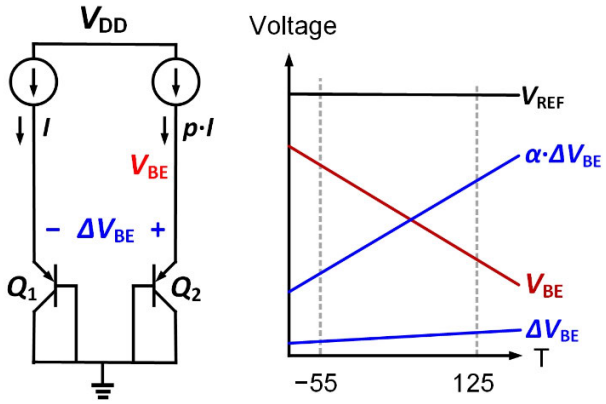

Fig. 1. Voltage-readout of a PNP-based front-end.

Fig. 1 illustrates the basic operating principle of a PNP-based temperature sensor. Two PNPs biased at a current ratio p are used to generate the following voltages:

$$V_{BE} = n_e \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right) \tag{1}$$

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = n_e \frac{kT}{q} \ln(p) \tag{2}$$

where n_e is the PNP's nonideality factor, k is the Boltzmann's constant, q is the unit electron charge, and I_C and I_S are the PNP's collector- and saturation-current, respectively. As shown in Fig. 1, the temperature dependence of the base–emitter voltage V_{BE} is complementary to absolute temperature (CTAT), while that of ΔV_{BE} is proportional to absolute temperature (PTAT). By multiplying ΔV_{BE} by a constant factor α and adding this to V_{BE}, a temperature-independent bandgap reference voltage can be made. This can then be used to generate a linear function of absolute temperature

$$\mu_{lin} = \frac{\alpha \cdot \Delta V_{BE}}{\alpha \cdot \Delta V_{BE} + V_{BE}} = \frac{\alpha \cdot \Delta V_{BE}}{V_{ref}}. \tag{3}$$

To achieve high accuracy, the spread in the various variables in (3) must be minimized. The spread in V_{BE}, which is mainly due to the spread of I_C and I_S, can be mitigated by a room-temperature PTAT trim [8], while offset errors in the readout of V_{BE} and ΔV_{BE} can be reduced to the microvolt-level by various combinations of chopping, auto-zeroing, and correlated double sampling [2], [3], [5]. The accurate implementation of the ratios α and p is also important. Their spread must typically be less than 0.01% to ensure

Manuscript received 1 March 2024; revised 28 April 2024 and 6 May 2024; accepted 14 May 2024. This article was approved by Associate Editor Taekwang Jang. This work was supported by Analog Devices Inc. (ADI). *(Corresponding author: Nandor G. Toth.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2024.3402131.

Digital Object Identifier 10.1109/JSSC.2024.3402131

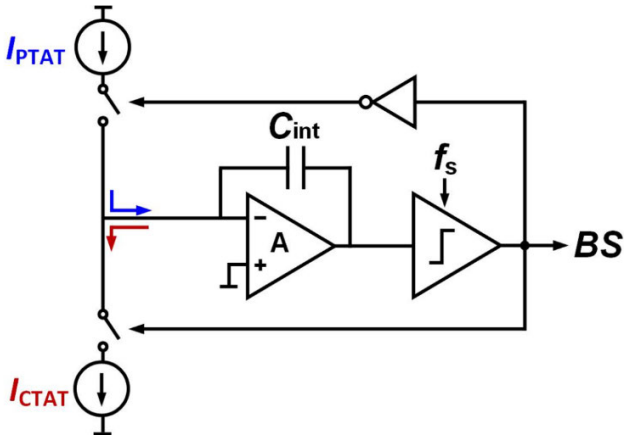


Fig. 2. Current-mode readout of a BJT-based temperature sensor.

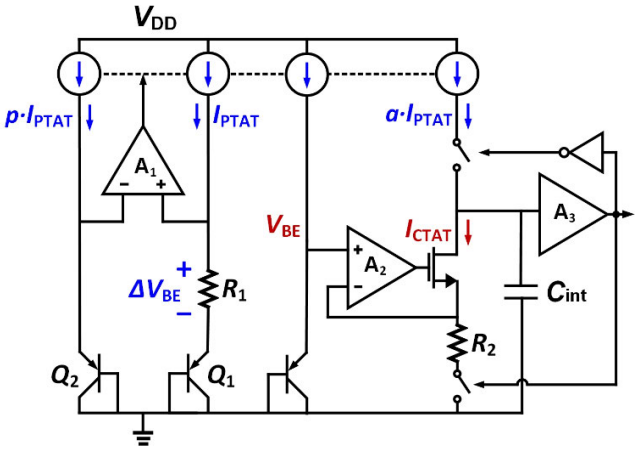


Fig. 3. Simplified schematic of the current-mode front-end used in [7].

that the resulting errors are less than 0.1 °C. In sensors based on SC $\Delta\Sigma$-modulators, α is usually defined by the ratio of the capacitors used to sample V_{BE} and ΔV_{BE}, respectively, while p is set by a current-mirror ratio. High accuracy can then be readily achieved with the help of dynamic element matching (DEM) [9]. Although the resolution of SC $\Delta\Sigma$-modulators is limited by kT/C noise, this can be mitigated by using large sampling capacitors and/or a large oversampling ratio (OSR). However, this comes at the expense of power and/or longer conversion times. As a result, their energy efficiency, as expressed by their resolution FoM [10], has remained stubbornly steady at around a few pJ·K^2 [1].

Alternatively, BJT-based sensors can be read out by CT $\Delta\Sigma$-modulators, which do not suffer from sampling noise [11]. However, their accuracy is often limited by the spread of α, since the effectiveness of DEM will now be limited by switching transients. In [6], which achieves a state-of-the-art resolution FoM of 0.19 pJ·K^2, α is determined by static resistor ratios. In [7], α is also defined by resistor ratios, but the use of a large resistor array and DEM results in an inaccuracy of $\pm$0.15 °C (3σ) from $-$45 °C to 130 °C, and a FoM of 3.6 pJ·K^2. In [12], α is defined by the gain of a capacitively-coupled instrumentation amplifier (CCIA). By calibrating this gain, an inaccuracy of $\pm$0.13 °C (3σ) from $-$55 °C to 125 °C is achieved, and a FoM of 5.4 pJ·K^2.

In this article, an extended version of [13], a PNP-based temperature sensor that achieves both high accuracy and energy efficiency is presented. Its readout architecture is based on a CT $\Delta\Sigma$-modulator that balances currents proportional to V_{BE} and ΔV_{BE}, respectively. Current-mirror and BJT mismatch is mitigated by DEM, while resistor-ratio mismatch is mitigated by a low-cost self-calibration scheme. As a result, the sensor achieves a FoM of 0.85 pJ·K^2 and an inaccuracy of $\pm$0.1 °C (3σ) from $-$55 °C to 125 °C after room-temperature calibration.

The rest of the article is organized as follows. Section II describes the operation of current-mode BJT-based temperature sensors and Section III discusses their design challenges. Section IV describes the design of the proposed sensor and its error-reduction techniques in detail. The circuit implementation is discussed in Section V. Section VI presents the measurement results and compares them to the state-of-the-art. The article ends with some conclusions.

II. Current-Mode Readout

Fig. 2 illustrates the basic operation of a PNP-based temperature sensor with a current-mode readout circuit. The temperature-dependent voltages, ΔV_{BE} and V_{BE}, are converted into the currents I_{PTAT} and I_{CTAT}, respectively, which are applied to a first-order CT $\Delta\Sigma$-modulator. Depending on the modulator's bitstream output (BS), either I_{CTAT} or I_{PTAT} will be integrated by a capacitor C_{int}. Over several cycles, the total integrated charge contributed by I_{CTAT} and I_{PTAT} will be balanced, and so the bitstream average μ will be a digital representation of temperature. As a result, $\mu \cdot I_{CTAT} = (1-\mu)\cdot I_{PTAT}$ and so $\mu = I_{PTAT}/(I_{CTAT}+I_{PTAT})$. As in (3), a linear function of temperature can then be obtained by appropriately scaling I_{PTAT} and I_{CTAT}.

A simplified schematic of the front-end of the design reported in [7], is shown in Fig. 3. $I_{PTAT} = \Delta V_{BE}/R_1$ is generated by using an opamp A_1 to force ΔV_{BE} over a resistor R_1, while $I_{CTAT} = V_{BE}/R_2$ is generated by using a second opamp A_2 to force V_{BE} over a second resistor R_2. These currents are then applied to the duty-cycle modulator formed by C_{int} and a Schmitt trigger A_3, whose output controls the DAC switches. By properly scaling the resistors, the duty cycle of the modulator's output will be a linear function of temperature. However, a high-frequency counter is required to digitize its duty-cycle modulated output. Furthermore, two low-offset high-gain opamps are required to accurately generate I_{PTAT} and I_{CTAT}.

A simpler front-end is shown in Fig. 4, which does not require an additional opamp to generate I_{CTAT}. As suggested in [14], I_{CTAT} is generated by applying V_{BE} to the positive terminal of the opamp (A_2) that also implements the first integrator of a current-balancing modulator. V_{BE} is then copied to its virtual ground and forced over R_2. Charge balancing is achieved by using the modulator's output BS to regulate I_{PTAT}. Although the bitstream average μ is not a linear function of temperature, it remains a linear function of $V_{BE}/\Delta V_{BE}$, as will be shown in Section IV, and so can be readily linearized in the digital backend [4].

III. Main Error Sources

In the target 180 nm process, the available PNPs are parasitic devices, which can only be biased via their emitters.

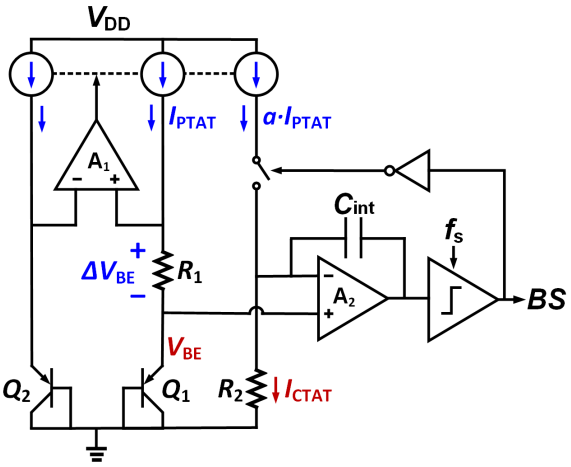


Fig. 4. Basic circuit diagram of the proposed front-end.

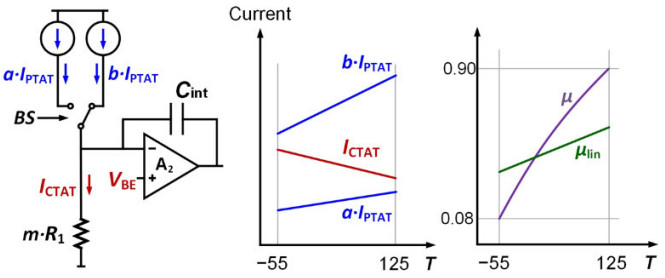


Fig. 5. Simplified circuit diagram with a dual-level IDAC, and the resulting currents versus temperature.

Their current gain β is low (∼3) and spreads, which decreases the accuracy of the resulting collector currents, and hence that of V_{BE} [15]. Taking the finite β of the PNPs into account, V_{BE} can be expressed as

$$V_{\mathrm{BE}} = n\frac{kT}{q}\ln\left(\frac{I_C}{I_S}\right) = n\frac{kT}{q}\ln\left(\frac{I_{\mathrm{PTAT}}}{I_S}\frac{\beta}{\beta+1}\right). \quad (4)$$

Although most of the spread in V_{BE} can be corrected by a PTAT trim [8], the temperature dependence of β will give rise to a residual error. Simulations show that this results in a worst-case corner spread of ±0.15 °C from −55 °C to 125 °C, which represents an upper bound on the sensor's inaccuracy. Since the relation between β and the collector current is quite constant, however, the collector-current ratio p (=7 in this work) is well-defined, and so the corresponding spread in ΔV_{BE} is only ±0.02 °C over the same temperature range.

As can be seen from Fig. 4, the voltage drop across R_1 is the sum of ΔV_{BE} and the input voltage of the bias amplifier A_1. As a result, both its finite dc gain A_{OL} and offset V_{os} will limit the accuracy of I_{PTAT} according to

$$I_{\mathrm{PTAT}} = \frac{\Delta V_{\mathrm{BE}} + V_{\mathrm{os}}}{R_1\left(1+\frac{1}{g_m R_1 A_{\mathrm{OL}}}\right)} \quad (5)$$

where g_m is the transconductance of the current source that biases $Q1$. For $p = 7$ and $g_m R_1 = 0.2$, $A_{\mathrm{OL}} > 77$ dB and $V_{\mathrm{os}} < 3$ μV are required to ensure that their respective error contributions are less than 0.01 °C (σ) at RT. In a similar manner, the input voltage of A_2 will cause errors in I_{CTAT}. To keep these below 0.01 °C (σ), $A_{\mathrm{OL}} > 65$ dB and $V_{\mathrm{os}} < 40$ μV are required. These requirements are more relaxed than those on A_1, since the temperature sensitivity of V_{BE} (−1.9 mV/K) is much larger than that of ΔV_{BE} (0.17 mV/K).

Errors in the collector current ratio p and the DAC current ratio a (see Fig. 4) cause errors in the PTAT current $I_{\mathrm{PTAT,ADC}}$ that is applied to the modulator

$$I_{\mathrm{PTAT,ADC}} = \frac{\Delta V_{\mathrm{BE}}}{R_1}\left(1+\frac{\Delta a}{a}+\frac{1}{\ln(p)}\frac{\Delta p}{p}\right). \quad (6)$$

Here $\Delta a/a$ and $\Delta p/p$ represent the mismatch in the respective current-mirror ratios. For an error of 0.01 °C (σ) at RT, $\Delta a/a < 60$ ppm (σ) and $\Delta p/p < 130$ ppm (σ) are required. Such tight matching cannot be achieved by good layout alone and thus necessitates the use of DEM or calibration. To make I_{CTAT} similarly accurate, $\Delta m/m < 60$ ppm (σ) is required, where m is the resistor ratio R_2/R_1. In this work, as will be discussed in the following section, it was decided to mitigate resistor-ratio errors by calibrating m rather than using DEM.

IV. Proposed Sensor Topology and Techniques

This section discusses the architectural choices and error-correction techniques used in this work. First, the design of the DAC and the choice of system coefficients are discussed. Then, the dynamic error-correction techniques necessary to achieve high accuracy are introduced, along with a novel scheme to calibrate the mismatch in R_2/R_1. Finally, the implementation of a voltage calibration scheme is discussed.

A. DAC Design and Coefficient Scaling

As shown in Fig. 4, a current-balancing readout can be implemented by using the BS of the CT ΔΣ-modulator to control a current-DAC that switches between 0 and I_{PTAT} to balance a continuous current I_{CTAT}. As shown in Fig. 5, however, better use of the modulator's dynamic range can be achieved by using a two-level current-DAC whose output switches between two levels: $a \cdot I_{\mathrm{PTAT}}$ and $b \cdot I_{\mathrm{PTAT}}$. With this scheme, the bitstream average μ can be expressed as

$$\mu = \frac{b}{b-a} - \frac{1}{(b-a)m}\cdot\frac{V_{\mathrm{BE}}}{\Delta V_{\mathrm{BE}}}. \quad (7)$$

With $p = 7$, the choice of $a = 1$, $b = 4$, and $m = 6$ results in a μ that varies in a non-linear fashion from 0.08 to 0.90 from −55 °C to 125 °C (see Fig. 5), and thus uses 82% of the modulator's dynamic range. With $X = V_{\mathrm{BE}}/\Delta V_{\mathrm{BE}}$, μ can then be expressed as

$$\mu = \frac{4}{3} - \frac{X}{18}. \quad (8)$$

Since μ is a linear function of X, a PTAT trim of V_{BE} can be implemented by performing a simple offset trim on μ in the digital domain [4]. As shown in Fig. 5, a linear function of temperature μ_{lin} can then be obtained by rewriting (3) as follows:

$$\mu_{\mathrm{lin}} = \frac{\alpha}{\alpha+X} = \frac{\alpha}{\alpha+24-18\mu}. \quad (9)$$

This can be converted into an output in °C by simply computing $D_{\mathrm{out}} = A \cdot \mu_{\mathrm{lin}} - B$, where A and B are fitting parameters.

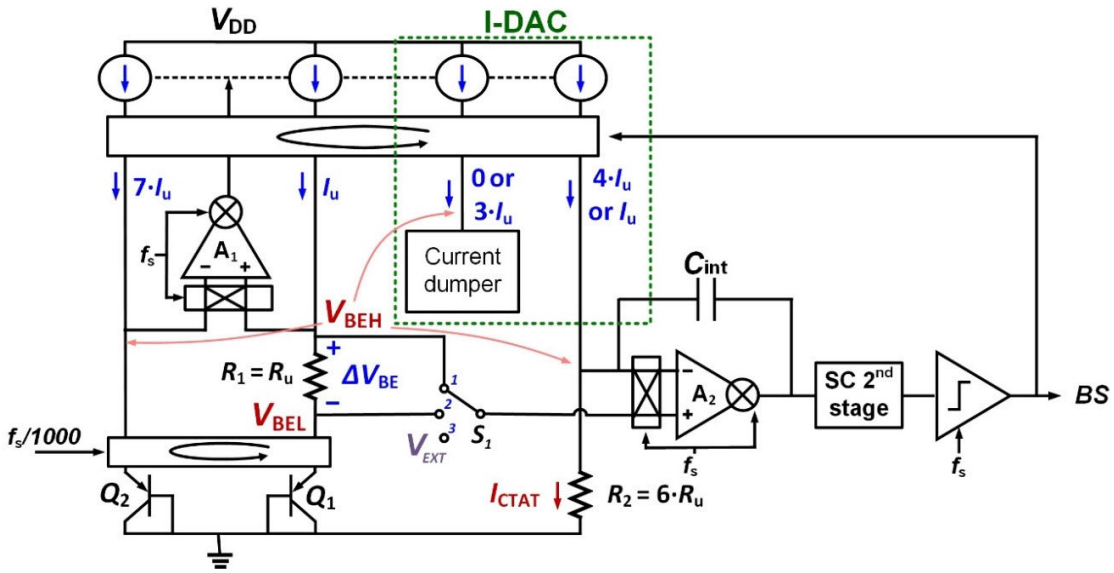


Fig. 6. Block diagram of the full sensor including dynamic error-correction techniques.

B. Dynamic Error-Reduction Techniques

A more detailed block diagram of the proposed sensor is shown in Fig. 6. The offset and $1/f$ noise of A_1 and A_2 are mitigated by chopping them at the sampling frequency f_s. Since the output spectrum of a $\Delta\Sigma$-modulator has notches at multiples of f_s, this choice of frequency prevents quantization noise folding.

As discussed in Section II, the current ratios p, a, and b should have errors below 100 ppm (σ). To realize this, the four current branches shown in Fig. 6 are implemented by 12-unit current sources, whose mismatch and $1/f$ noise are mitigated by DEM. One unit source biases Q_1, seven bias Q_2, while 4 are used to implement the two-level DAC. To avoid intermodulation between the bitstream and the DEM sequence, a bitstream-controlled (BSC) DEM scheme is employed [16]. As shown in Fig. 7, this involves the use of two barrel-shifting registers to control the DEM switches: one which is clocked when BS $= 0$ (SR_0) and one which is clocked when BS $= 1$ (SR_1). In this way, each DEM state occurs with equal frequency, irrespective of the bitstream sequence, thus avoiding quantization noise folding.

The mismatch between the two PNPs, which would otherwise cause spread to ΔV_{BE}, is also mitigated by DEM. Since their $1/f$ noise corner is well below 10 Hz, they are swapped at $f_s/1000$, which results in negligible quantization noise folding.

C. Transient Error Reduction

In a CT $\Delta\Sigma$-modulator, the switching transients of the DAC will also be integrated by the first stage, which may cause significant errors and ISI. To minimize such transients, unused DAC elements are switched to V_{BEH} by connecting them to a BJT-based current dumper (see Fig. 6). Since the virtual grounds of A_1 and A_2 are also at V_{BEH}, all 12 current sources are switched between the same voltage levels, which further minimizes DEM-related switching transients.

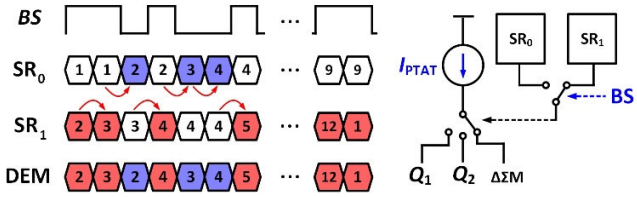


Fig. 7. Implementation of BSC DEM.

D. Resistor Ratio Calibration

As discussed in Section III, the error in the resistor ratio $m = R_2/R_1$ should be less than 100 ppm (σ), which cannot be achieved by precise layout alone. This would be difficult to achieve with DEM, since the voltage drops across R_1 and R_2 are quite different, leading to large switching transients during DEM transitions due to the charging and discharging of their parasitic capacitances. In this work, resistor mismatch is mitigated by digitizing m and then correcting its spread in the digital domain. This is done by performing two conversions with the first integrator's virtual ground connected to either V_{BEL} or $V_{\mathrm{BEL}} + \Delta V_{\mathrm{BE}}$ (see Fig. 6). The difference $\Delta\mu$ in the resulting bitstream averages is then

$$\Delta\mu = \frac{1}{m(b-a)} \frac{(V_{\mathrm{BEL}} + \Delta V_{\mathrm{BE}}) - V_{\mathrm{BEL}}}{\Delta V_{\mathrm{BE}}} = \frac{1}{m(b-a)} \quad (10)$$

where b and a are current ratios, whose accuracy is guaranteed by DEM. As a result, the resistor ratio m can be accurately determined. Any mismatch can then be digitally corrected with the help of the following equation:

$$\mu_{\mathrm{calibrated}} = \frac{\mu - \frac{4}{3}}{18 \cdot \Delta\mu} + \frac{4}{3}. \quad (11)$$

However, (10) only holds if V_{BE} and ΔV_{BE} are constant during the two conversions, which in turn means that both thermal noise and ambient temperature drift will cause calibration errors. Detecting mismatch errors below 100 ppm requires the

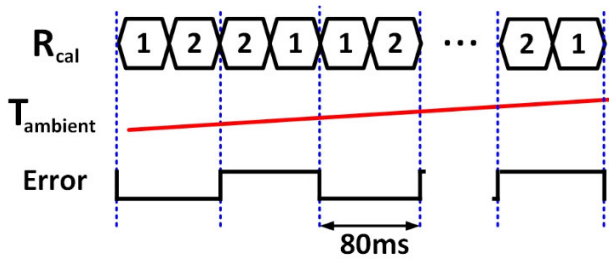


Fig. 8. Alternating differential resistor-calibration measurement.

ambient temperature to be stable to within 1.5 mK, and the modulator's resolution to be below 0.5 mK (σ). To relax the stringent requirements on temperature stability, the calibration is split up into ten pairs of short (40 ms) conversions, which are performed in alternating order, as shown in Fig. 8. This method cancels $\Delta\mu$ errors caused by linear temperature drift. The resistor ratio can then be determined in 0.8 s without an external reference, making it a low-cost calibration.

E. Voltage Calibration

As described in [17], voltage calibration is a low-cost alternative to a temperature trim. It involves digitizing ΔV_{BE} by performing a $\Delta\Sigma$-conversion in which V_{BE} is replaced by a known external voltage V_{EXT}, which is chosen to be approximately equal to the expected V_{BE} (see Fig. 6). The exact temperature of the die can then be determined from (2) and used to perform a temperature trim.

The accuracy of voltage calibration is limited by the spread in the PNP's nonideality factor (n_e), which causes errors in the temperature estimated from ΔV_{BE}. However, compared to a traditional temperature trim, in which an external temperature sensor must be brought into thermal equilibrium with the die, this scheme only requires a voltage reference and can be performed in two conversions (80 ms), making it a fast and low-cost trimming technique.

V. Circuit Implementation

A. Front-End

A more detailed schematic of the proposed front-end is shown in Fig. 9. As discussed above, DEM is used to mitigate the mismatch of the PNPs and the PMOS current sources. To avoid bias current errors due to the IR drops across the DEM switches, Kelvin connections are used to connect PNP/R_1 pairs to the current sources and the bias opamp A_1 [7]. A multiplexer is then used to connect the appropriate V_{BE} to the modulator, depending on the DEM (S_{DEM}) and R_{CAL} states. The emitter-current ratio $p = 7$ is established by 8 cascoded PMOS current sources, which are biased in strong inversion ($g_m/I_D = 4$) to maximize their initial matching and reduce their thermal noise contribution to I_{PTAT} [18]. Their high r_{out} (>40 GΩ at RT) ensures that small changes in their drain voltages, as occur during resistor and voltage calibration, result in negligible current errors. As discussed above, the current sources are then incorporated in a BSC-DEM scheme, which ensures that the error due to their residual mismatch is negligible (<5 mK). This is implemented by connecting each of the current sources to a 1:4 multiplexer.

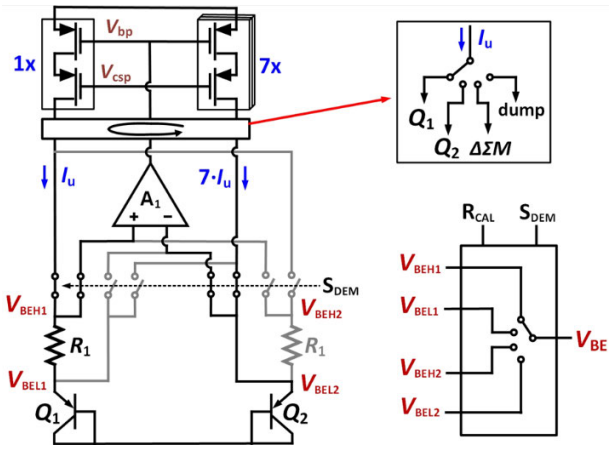


Fig. 9. Circuit diagram of the front-end and the V_{BE} switches.

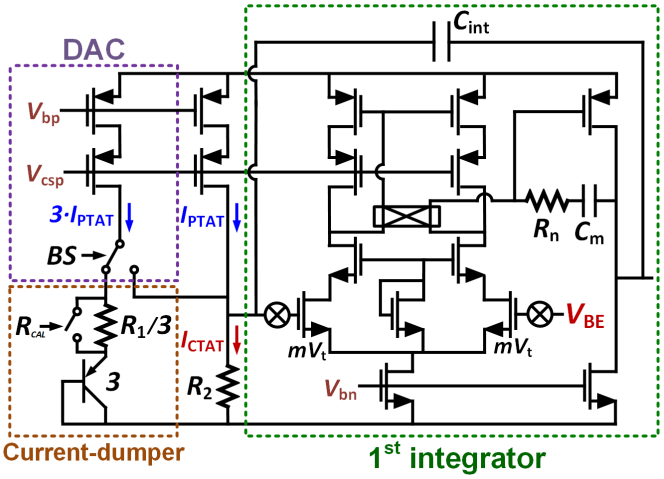


Fig. 10. Circuit diagram of the DAC and first integrator.

Opamp A_1 is implemented as an energy-efficient telescopic amplifier with an NMOS input pair. Its tail current is $6{\cdot}I_{\mathrm{PTAT}}$, which ensures that its thermal noise contribution to I_{PTAT} is similar to that of R_1. The amplifier has an A_{OL} of 83 dB over PVT, which satisfies the requirements described in Section II. Furthermore, it has a GBW of 220 kHz at RT, which ensures that the error due to switching transients is below 30 mK.

B. ΔΣM

A current-input CT-ΔΣ modulator is used to digitize the signals in the front-end. A second order loop filter is implemented for a good compromise between the required OSR and design complexity. The ΔΣM is clocked at 50 kHz over a conversion time of 40 ms, realizing an OSR of 2000. This ensures that the quantization noise power is at least 10 dB lower than the thermal noise power over the temperature range.

Fig. 10 shows a circuit diagram of the implemented DAC and first integrator. Both the DAC and the first integrator reuse the PTAT current generated in the front end. The current dumper consists of three parallel PNPs in series with a resistor $R_1/3$ that is shorted during resistor calibration. In this way,

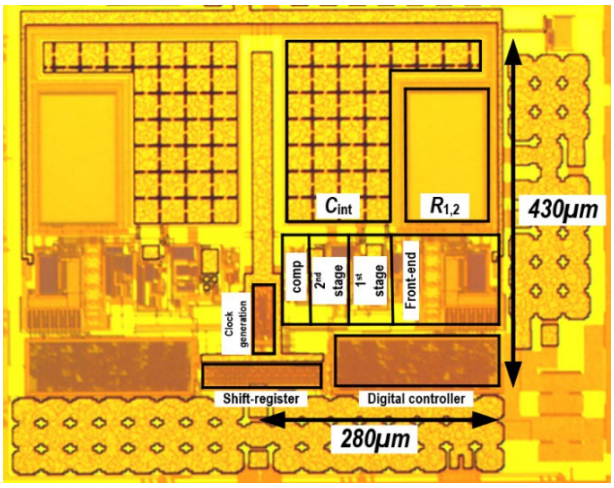


Fig. 11. Micrograph of the die.

the dumper voltage is set to V_{BEH} and V_{BEL} during normal operation and resistor calibration, respectively.

The first integrator's OTA must source/sink the output current of the DAC, while also providing high dc gain and GBW. To achieve this, it was realized by a two-stage Miller-compensated amplifier. Like A_1, the first stage is a chopped telescopic cascode amplifier. Both A_1 and A_2 use input pairs based on medium-V_t NMOS devices to ensure that their tail transistors remain in saturation at high temperatures, when their input common-mode voltage (=V_{BEH}) is low (~450 mV). Since A_2 has relaxed noise requirements, the current in the first stage of A_2 is 3× lower than in A_1. The second stage is a PMOS common-source stage biased at $4.5 \cdot I_{\mathrm{PTAT}}$. The OTA has an A_{OL} of >110 dB over PVT and a GBW of 600 kHz, which ensure that errors due to switching transients are below 20 mK. It is stabilized by a Miller capacitor C_m (=680 fF) and a nulling resistor R_n (=165 kΩ). The current signals are integrated on C_{int} (=60 pF), which ensures that the voltage swing at the output of A_2 is less than 0.6 V over PVT.

The second integrator is an area-efficient SC circuit, whose kT/C noise is attenuated by the high voltage gain of the first integrator. It dissipates 4× less power and occupies 11× less area than the first integrator.

VI. Measurement Results

The proposed temperature sensor was fabricated in a standard 0.18 μm CMOS process. Two sensors were realized on each die, thus enabling the use of differential measurements to cancel ambient temperature drift [19]. As shown in Fig. 11, each sensor occupies 0.12 mm^2, most of which is taken up by capacitors and resistors. All digital control signals are generated on-chip from a 200 kHz primary clock. For flexibility, the nonlinearity removal and sinc^2 decimation filter are implemented off-chip.

A. Power Consumption

Each sensor draws 9.5 μA from a 1.7 V supply. Fig. 12 shows a breakdown of the corresponding power dissipation, with f_s = 50 kHz. The front end dissipates the most power,

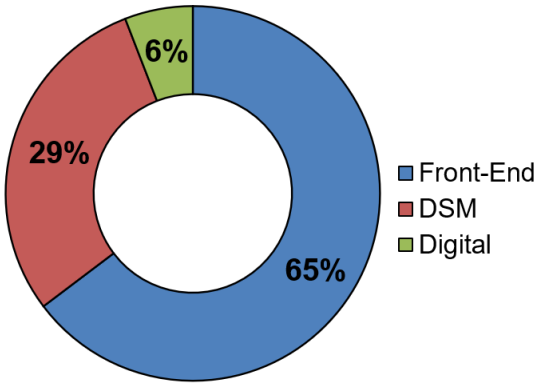


Fig. 12. Power distribution of a sensor.

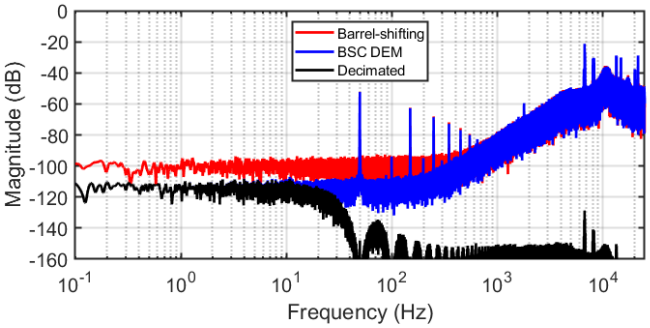


Fig. 13. FFT of the bitstream.

followed by the ΔΣM, and the digital logic. A version of the sensor with an on-chip decimation filter, a polynomial-based nonlinearity removal, and an SPI interface were also made [5]. The required digital circuitry occupies 0.04 mm^2 and dissipates 0.98 μA at RT, increasing the area and power by 33% and 10%, respectively.

B. FFT and Resolution

Fig. 13 shows an FFT of the bitstream when the modulator is operating in free-running mode. It exhibits second order quantization noise shaping, with a $1/f$ noise corner well below 100 mHz. Compared to the use of barrel-shifting DEM, the use of BSC-DEM does a better job of mitigating quantization noise folding. The remaining in-band tones are due to the BJT DEM and are suppressed by the notches of the sinc^2 decimation filter. As can be seen in Fig. 14, the sensor becomes quantization noise limited for conversions shorter than 10 ms. It achieves a thermal-noise limited resolution of 1.1 mK (rms) in 40 ms, resulting in a resolution figure of merit (FoM) of 0.85 pJ·K^2.

C. Extracted Resistor Ratios

Fig. 15 shows a histogram of the normalized resistor ratio of all 40 measured samples. Its spread has a standard deviation of 450 ppm, which agrees well with mismatch simulations. These indicate that to achieve the required 60 ppm (σ) mismatch, a resistor area of 1.6 mm^2 would have been required, thus validating the use of resistor-ratio calibration.

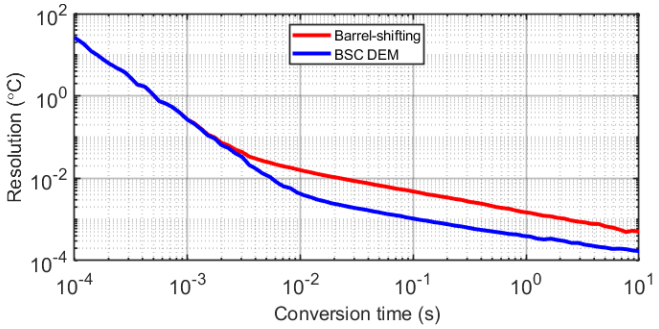


Fig. 14. Temperature resolution plotted versus conversion time.

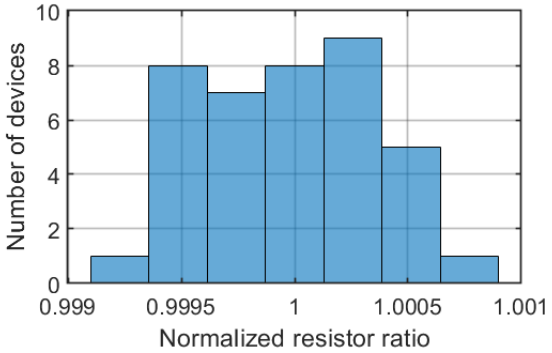


Fig. 15. Histogram of the normalized resistor ratios extracted from 40 sensors.

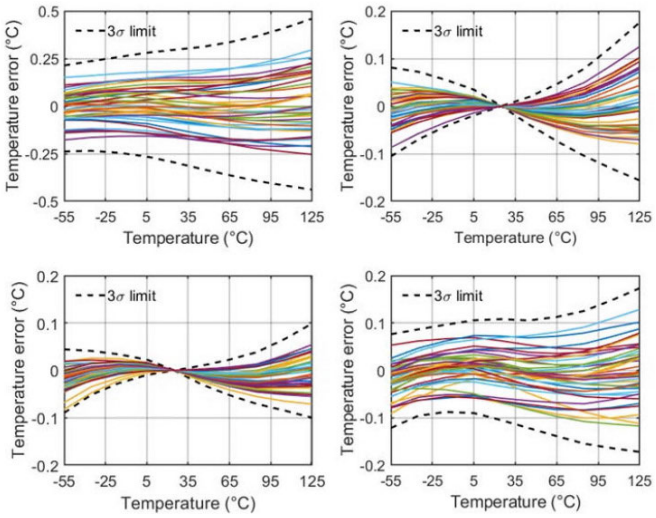


Fig. 16. Temperature spread of 40 sensors before trimming (top left), with RT trim (top right), with RT trim and resistor-ratio calibration (bottom left), with voltage- and resistor-ratio calibration (bottom right).

D. Accuracy Measurements

To determine the sensor's accuracy, 40 sensors on 20 dies were characterized in a temperature-controlled oven, with the samples mounted in close thermal contact with a calibrated pt-100 thermistor. The batch-calibrated inaccuracy using the linearization technique discussed in Section IV-A is shown in Fig. 16 (top left). The sensor achieves an inaccuracy of ±0.45 °C (3σ), with a residual nonlinearity of ±0.015 °C ($\alpha \approx 11.44$). This improves to ±0.17 °C (3σ) after a RT trim (see Fig. 16, top right). After applying resistor-ratio calibration, the target inaccuracy of ±0.1 °C (3σ) is achieved (see Fig. 16, bottom left). Replacing the temperature trim with low-cost voltage calibration increases the inaccuracy to ±0.17 °C (3σ) (see Fig. 16, bottom right), which is sufficient for many applications. Table I summarizes the effectiveness of each

TABLE I
ACCURACY-IMPROVEMENT TECHNIQUES

CHOP	CM DEM	BJT DEM	R-CAL	Trimmed Inacc. (3σ)[1]
OFF	ON	ON	ON	±8.5°C
ON	**OFF**	ON	ON	±4.0°C
ON	ON	**OFF**	ON	±0.37°C
ON	ON	ON	**OFF**	±0.15°C
ON	ON	ON	ON	±0.10°C

[1]12 samples

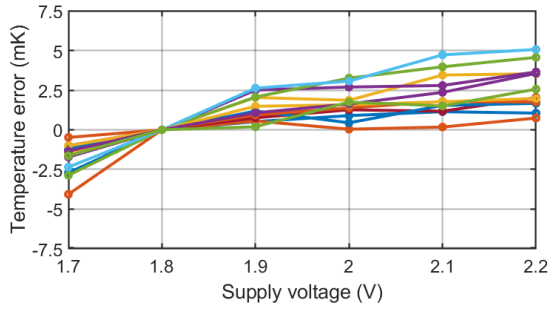


Fig. 17. Power supply sensitivity of 12 samples.

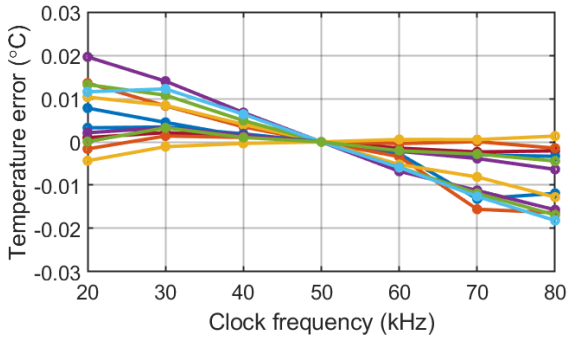


Fig. 18. Clock frequency sensitivity of 12 samples.

TABLE II
BATCH TO BATCH VARIATION OF THE SENSOR AND BATCH CALIBRATION PARAMETERS

Parameters	Batch 1	Batch 2
A	690.723	691.017
B	287.088	287.093
α	11.44	11.44
n_e	1.00538	1.00532
Untrimmed Inaccuracy	±0.45°C	±0.78°C
1-pt. Trimmed Inaccuracy	±0.10°C	±0.10°C
Voltage-Calibrated Inaccuracy	±0.17°C	±0.22°C

TABLE III
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

	JSSC'17 [4]	**SSCL'22** [20]	**ISSCC'14** [7]	**ASSCC'19** [12]	**ISSCC'23** [5]	**ISSCC'20** [6]	**This work**
Sensor type	PNP	NPN	PNP	NPN	PNP	NPN	**PNP**
Architecture	DTΔΣM	DTΔΣM	DCM	CTΔΣM	DTΔΣM	CTΔΣM	**CTΔΣM**
Technology	0.16µm	0.18µm	0.18µm	0.18µm	0.18µm	0.11µm	**0.18µm**
Chip area [mm²]	0.16	0.058	0.8	0.35	0.25	0.2	**0.12**
Supply current [µA]	4.6	0.17	55	5.5	0.81	550	**9.5**
Supply voltage [V]	1.5 to 2	1.25	1.25	1.6 to 2.2	0.95 to 1.4	1.125	**1.7 to 2.2**
Supply sensitivity [°C/V]	0.01	0.07	0.1	0.01	0.2	-	**0.01**
Temperature range	-55°C to 125°C	-15°C to 85°C	-45°C to 130°C	-40°C to 125°C	-55°C to 125°C	-35°C to 95°C	**-55°C to 125°C**
3σ Inaccuracy [°C] after a 1-pt trim	±0.06[2]	±0.15	±0.15[2]	±0.13[2,3]	±0.15	-	**±0.1**
Relative inaccuracy [%]	0.07	0.3	0.17	0.16	0.17	-	**0.11**
Resolution [mK]	15	15	3	1.67	1.8	0.65	**1.1**
Conversion time [ms]	5	50	2.2	218	128	0.72	**40**
Resolution FoM[1] [pJK²]	7.8	2.3	3.6	5.4	0.34	0.19	**0.85**

[1] FoM = Energy / Conversion x (Resolution)² [2]After systematic non-linearity removal [3]After ADC gain and offset calibration

accuracy improvement technique on the trimmed inaccuracy of 12 samples. Among all the techniques applied, chopping shows the largest improvement, followed by current mirror DEM and BJT DEM, respectively. Resistor-ratio calibration has a small, but still significant, effect on the measured inaccuracy.

E. Power Supply and Clock Frequency Sensitivity

Fig. 17 shows the power supply sensitivity at RT of 12 samples as V_{DD} varies from 1.7 to 2.2 V. The average PSS is 0.01 °C/V, which is at par with the state-of-the-art.

Fig. 18 shows the sensor's sensitivity at RT to changes in clock frequency. As the clock frequency increases from 20 to 80 kHz, its sensitivity to switching transients increases. An average clock frequency sensitivity of 0.3 mK/kHz is found, which indicates that switching-transient related errors were successfully minimized.

F. Batch-to-Batch Measurements

The batch-to-batch accuracy was investigated by measuring sensors from different wafers and applying the same batch coefficients. Using the coefficients from batch 1 (α, A, and B) results in a maximum untrimmed inaccuracy of ±0.95 °C (3σ) (see Fig. 19, top), which improves to 0.14 °C after resistor-ratio calibration and a RT trim (see Fig. 19, middle). Replacing the temperature trim with voltage calibration using the non-ideality factor (n_e) obtained from batch 1 results in a maximum batch-to-batch inaccuracy (3σ) of 0.22 °C (see Fig. 19, bottom). Table II shows the optimized batch parameters for both batches and the resulting inaccuracies. Averaging these parameters and applying them to both batches results in worst-case untrimmed, trimmed, and voltage-calibrated inaccuracies (3σ) of 0.65 °C, 0.12 °C, and 0.20 °C, respectively.

G. Comparison to the State-of-the-Art

Table III summarizes the performance of the proposed sensor and compares it with that of other state-of-the-art

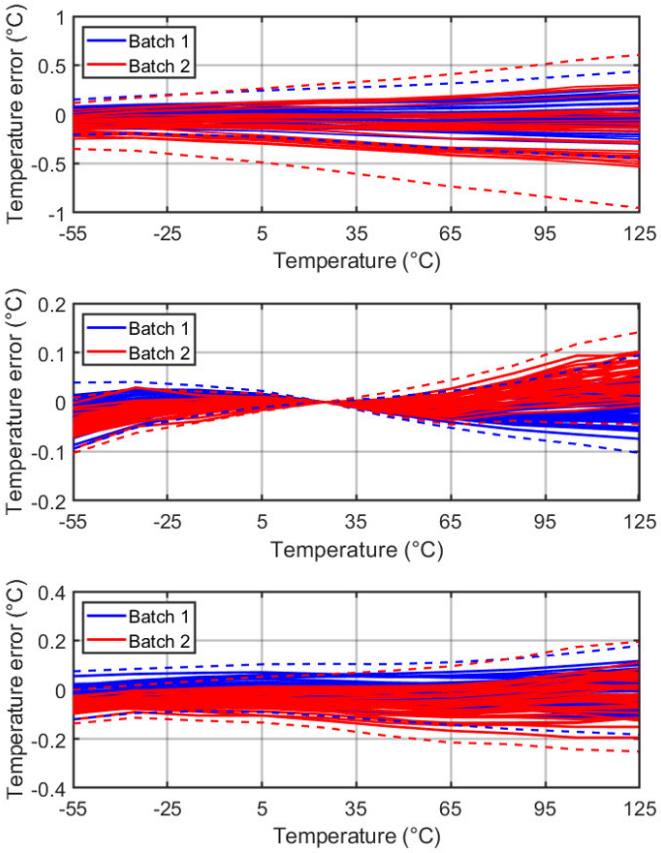


Fig. 19. Untrimmed inaccuracy of 2 batches (top), after resistor calibration and a temperature trim (middle), and after resistor- and voltage-calibration (bottom).

BJT-based temperature sensors that achieve similar accuracy (RIA $<$ 0.2%) and/or energy efficiency [1]. The proposed sensor demonstrates excellent all-around performance, achieving both high accuracy and energy efficiency (see Fig. 20), while also achieving state-of-the-art power supply sensitivity and occupying only a small area.

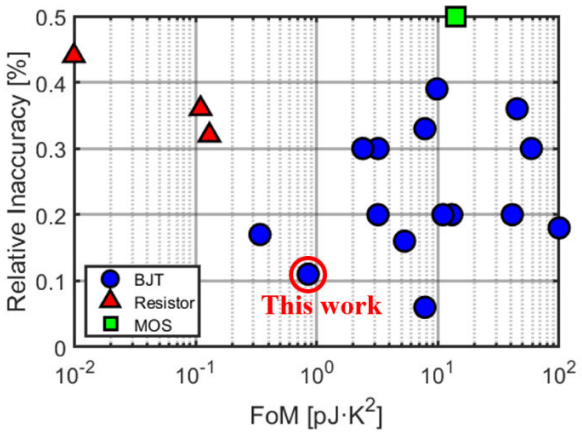


Fig. 20. FoM versus RIA after a 1-pt trim for state-of-the-art CMOS temperature sensors.

VII. Conclusion

This work proposes a current-mode BJT-based temperature sensor employing a CT readout. The front-end and readout circuits were designed to achieve high energy efficiency. High accuracy is achieved by employing chopping and DEM to mitigate component mismatch, as well as a novel resistor-ratio self-calibration technique. Fabricated in a 0.18 μm process, the sensor occupies 0.12 mm^2 and draws 9.5 μA from a 1.7 V supply. It achieves a resolution FoM of 0.85 pJ·K^2 and a 1-point trimmed inaccuracy of 0.1 °C (3σ) from −55 °C to 125 °C. This performance makes the sensor competitive with the state-of-the-art in terms of area, power supply sensitivity, energy efficiency, and accuracy.

Acknowledgment

The authors would like to thank Lukasz Pakula and Zu-Yao Chang for their measurement support.

References

[1] K. A. A. Makinwa. *Smart Temperature Sensor Survey*. Accessed: Aug. 2023. [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls

[2] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ±0.1 °C from −55 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 12, no. 40, pp. 2805–2815, Dec. 2005.

[3] K. Souri, Y. Chae, and K. A. A. Makinwa, "A CMOS temperature sensor with a voltage-calibrated inaccuracy of ±0.15 °C (3σ) from −55 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 292–301, Jan. 2013.

[4] B. Yousefzadeh, S. H. Shalmany, and K. A. A. Makinwa, "A BJT-based temperature-to-digital converter with ±60 mK (3σ) inaccuracy from −55 °C to +125 °C in 0.16-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1044–1052, Apr. 2017.

[5] Z. Tang, S. Pan, and K. A. A. Makinwa, "23.5 A sub-1 V 810 nW capacitively-biased BJT-based temperature sensor with an inaccuracy of ±0.15 °C (3σ) from −55 °C to 125 °C," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 22–24.

[6] S. H. Shalmany et al., "A 620 μW BJT-based temperature-to-digital converter with 0.65 mK resolution and FoM of 190fJ·K^2," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 70–72.

[7] A. Heidari, G. Wang, K. A. A. Makinwa, and G. Meijer, "A BJT-based CMOS temperature sensor with a 3.6pJ·K^2-resolution FoM," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 224–225.

[8] G. C. M. Meijer, "An IC temperature transducer with an intrinsic reference," *IEEE J. Solid-State Circuits*, vol. SSC-15, no. 3, pp. 370–373, Jun. 1980.

[9] R. J. Van De Plassche, "Dynamic element matching for high-accuracy monolithic D/A converters," *IEEE J. Solid-State Circuits*, vol. SSC-11, no. 6, pp. 795–800, Dec. 1976.

[10] K. A. A. Makinwa, "Smart temperature sensors in standard CMOS," *Procedia Eng.*, vol. 5, pp. 930–939, Jan. 2010.

[11] M. Pertijs, A. Niederkorn, X. Ma, B. McKillop, A. Bakker, and J. Huijsing, "A CMOS temperature sensor with a 3σ inaccuracy of ±0.5 °C from −50 °C to 120 °C," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers. ISSCC.*, 2003, pp. 200–488.

[12] R. K. Kumar, H. Jiang, and K. A. A. Makinwa, "An energy-efficient BJT-based temperature-to-digital converter with ±0.13 °C (3σ) inaccuracy from −40 to 125 °C," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2019, pp. 107–108.

[13] N. G. Toth, Z. Tang, T. Someya, S. Pan, and K. A. A. Makinwa, "A BJT-based temperature sensor with ±0.1 °C(3σ) inaccuracy from −55 °C to 125 °C and a 0.85pJ·K^2 resolution FoM using continuous-time readout," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Paper*, Feb. 2023, pp. 358–360.

[14] M. Eberlein and H. Pretl, "A current-mode temperature sensor with a ±1.56 °C raw error and duty-cycle output in 16 nm FinFET," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5.

[15] M. A. Pertijs and J. H. Huijsing, *Precision Temperature Sensors in CMOS*. Dordrecht, The Netherlands: Springer, 2006.

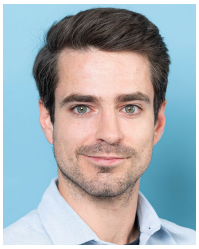
[16] M. A. Pertijs and J. H. Huijsing, "A sigma-delta modulator with bitstream-controlled dynamic element matching," in *Proc. 30th Eur. Solid-State Circuits Conf.*, Sep. 2004, pp. 187–190.

[17] M. A. P. Pertijs, A. L. Aita, K. A. A. Makinwa, and J. H. Huijsing, "Voltage calibration of smart temperature sensors," in *Proc. IEEE Sensors*, Oct. 2008, pp. 756–759.

[18] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.

[19] S. Pan and K. A. A. Makinwa, "A 0.25 mm^2-resistor-based temperature sensor with an inaccuracy of 0.12 °C (3σ) from −55 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3347–3355, Dec. 2018.

[20] T. Someya, V. van Hoek, J. Angevare, S. Pan, and K. Makinwa, "A 210 nW NPN-based temperature sensor with an inaccuracy of ±0.15 °C (3σ) from −15 °C to 85 °C utilizing dual-mode frontend," *IEEE Solid-State Circuits Lett.*, vol. 5, pp. 272–275, 2022.



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