Low-Power CMOS Smart Temperature Sensor With a Batch-Calibrated Inaccuracy of ±0.25 °C (±3σ) from −70 °C to 130 °C

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***Abstract*— In this paper, a low-power CMOS smart temperature sensor is presented. The temperature information extracted using substrate PNP transistors is digitized with a resolution of 0.03 °C using a precision switched-capacitor (SC) incremental ΔΣ A/D converter. After batch calibration, an inaccuracy of ±0.25 °C (±3σ) from −70 °C to 130 °C is obtained. This represents a two-fold improvement compared to the state-of-the-art. After individual calibration at room temperature, an inaccuracy better than ±0.1 °C over the military temperature range is obtained, which is in-line with the state-of-the-art. This performance is achieved at a power consumption of 65 μW during a measurement time of 100 ms, by optimizing the power/inaccuracy tradeoffs, and by employing a clock frequency proportional to absolute temperature. The latter ensures accurate settling of the SC input stage at low temperatures, and reduces the effects of leakage currents at high temperatures.**

***Index Terms*— ΔΣ A/D conversion, batch calibration, smart temperature sensors, substrate PNP transistors.**

I. Introduction

SMART temperature sensors based on the substrate PNP transistors available in standard CMOS technology can achieve inaccuracies below ±0.1 °C over the military range (from −55 °C to 125 °C) [1], [2]. To achieve this, such sensors require individual calibration and trimming. Although efficient methods of calibration and trimming have been devised [3], [4], individual calibration is still a significant cost contributor, even if it is only done at room temperature. Significant cost reductions can be achieved by employing batch calibration, i.e. calibrating a limited number of samples from a production batch, obtaining an estimate of their average error, and then using this information to trim the entire batch.

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In this work, a CMOS temperature sensor is presented that employs batch calibration to achieve an inaccuracy of ±0.25 °C (±3σ) from −70 °C to 130 °C, which represents a two-fold improvement on the state-of-the-art [1], [5]. Moreover, the sensor achieves an inaccuracy of ±0.1 °C after individual calibration at room temperature, at par with the state-of-the-art [1], while consuming 3 times less energy per measurement. While more energy-efficient temperature sensors have been reported [5], [6], this is at the expense of somewhat lower accuracy.

This paper is organized as follows. Section II reviews the sensor's operating principle, and discusses the main sources of inaccuracy. Section III describes the sensor front-end at the circuit level, detailing the approach taken to achieve the combination of high accuracy and low energy consumption. Section IV addresses innovative aspects of the incremental ΔΣ A/D converter, including a power-efficient implementation of its first integrator, and the use of a clock frequency proportional to absolute temperature (PTAT) to widen the sensor's temperature range. Measurement results are presented and discussed in Section V, followed by conclusions.

II. Sensor Operating Principle

A. Sensor Block Diagram

Fig. 1 shows a block diagram of the sensor, which consists of a front-end circuit, a ΔΣ modulator and a decimation filter. In the front-end circuit, a substrate PNP transistor, either Q_L or Q_R, biased through its emitter with a current I_{bias}, generates a voltage V_{BE}, complementary to absolute temperature (CTAT), given by

$$V_{BE}(T) = \frac{kT}{q}\ln\left(\frac{I_C(T)}{I_S(T)}+1\right) \approx \frac{kT}{q}\ln\left(\frac{I_{bias}(T)}{I_S(T)}\right) \quad (1)$$

where k is Boltzmann's constant, T the absolute temperature, q the electron charge and I_S is the transistor's saturation current. The approximation is valid for $I_C \approx I_E = I_{bias}$ and if the ratio $I_C/I_S \gg 1$.

A voltage proportional to absolute temperature (PTAT) $\Delta V_{BE}(T) = V_{BE,R} - V_{BE,L}$, is obtained by biasing two nominally equal PNP transistors Q_L and Q_R at a 1:m current ratio, i.e. $m = I_{bias,R}/I_{bias,L}$. Provided the approximation in (1)

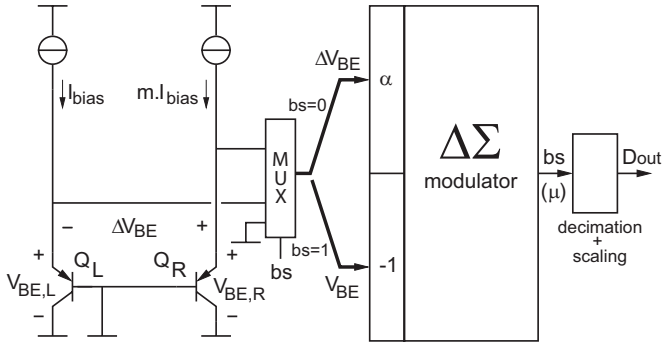

Fig. 1. Sensor block diagram. The front-end generates V_{BE} and ΔV_{BE} that are multiplexed into the $\Delta\Sigma$ modulator to produce a bitstream bs. A digital reading of temperature D_{out} is available after decimation/scaling.

is valid and mismatch errors in the bias currents and PNP transistors are negligible, this PTAT voltage, given by

$$\Delta V_{\mathrm{BE}}(T) = \frac{kT}{q}\ln(m) \tag{2}$$

is intrinsically accurate. Ideally, it does not depend on any processing parameters [7] and, because of that, hardly suffers from process spread.

By adding to either $V_{\mathrm{BE,L}}$ or $V_{\mathrm{BE,R}}$ an amplified version of ΔV_{BE}, i.e. $\alpha\Delta V_{\mathrm{BE}}$, a first-order temperature-independent reference voltage V_{REF} is obtained

$$V_{\mathrm{REF}} = \alpha\Delta V_{\mathrm{BE}} + V_{\mathrm{BE}} \tag{3}$$

where α is the scale factor required to compensate for the variation of V_{BE} with the temperature, about -2 mV/° C, with the variation of ΔV_{BE} with the temperature, about $+0.14$ mV/° C for $m = 5$. Exact values for α were obtained through simulations, taking into account the actual front-end biasing and PNP emitter areas (where measured data from a previous design [1] was used to obtain an accurate simulation model).

The temperature can thus be measured ratiometrically by comparing the scaled PTAT voltage $\alpha\Delta V_{\mathrm{BE}}$ with the reference voltage V_{REF} [8], i.e., by evaluating the ratio $\mu = V_{\mathrm{PTAT}}/V_{\mathrm{REF}}$

$$\mu = \frac{V_{\mathrm{PTAT}}}{V_{\mathrm{REF}}} = \frac{\alpha\Delta V_{\mathrm{BE}}}{\alpha\Delta V_{\mathrm{BE}} + V_{\mathrm{BE}}} = \frac{\alpha\frac{kT}{q}\ln(m)}{\alpha\frac{kT}{q}\ln(m) + V_{\mathrm{BE}}} \tag{4}$$

which is also PTAT.

Whereas the front-end generates V_{BE} and ΔV_{BE}, the $\Delta\Sigma$ modulator generates a bitstream bs, whose average equals μ. This is achieved through charge balancing, i.e. by properly applying, every clock cycle, either $\alpha\Delta V_{\mathrm{BE}}$ (when $bs = 0$) or $\alpha\Delta V_{\mathrm{BE}} - V_{\mathrm{REF}} = -V_{\mathrm{BE}}$ (when $bs = 1$) to the input of a loop-filter [1]. Because of the modulator's feedback, the average at the input of the loop filter over time is zero, and the output bitstream bs will have the desired average μ given by (4). After decimation, the temperature reading can then be determined as

$$D_{\mathrm{out}} = A\mu + B \tag{5}$$

where $A \approx 600$ and $B \approx -273$ are the gain and offset coefficients, respectively, for a direct result in degrees Celsius.

B. Design Approach

In order to design a low-power high-accuracy sensor, the minimum amount of power needed to minimize the various error sources must be determined. To find how each error affects the temperature measurement, the sensitivity of the measured temperature (as given in (5)) to changes in V_{BE}, ΔV_{BE}, α [8] and m is calculated. These sensitivities are equal to:

$$\begin{aligned}
\frac{\partial V_{\mathrm{BE}}}{\partial T} &\cong 3\frac{\mathrm{mV}}{^{\circ}\mathrm{C}} \\
\frac{\partial \Delta V_{\mathrm{BE}}}{\partial T} &\cong \frac{3}{\alpha}\frac{\mathrm{mV}}{^{\circ}\mathrm{C}} \\
\frac{1}{\alpha}\frac{\partial \alpha}{\partial T} &\cong \frac{2}{300}\frac{1}{^{\circ}\mathrm{C}} \\
\frac{1}{m}\frac{\partial m}{\partial T} &\cong \frac{0.15}{\alpha}\frac{1}{^{\circ}\mathrm{C}}.
\end{aligned} \tag{6}$$

Allocating a maximum error contribution of 0.01 °C to each of the error sources, to arrive at an overall error below 0.1 °C, a worst case variation of about 30 μV in V_{BE}, 2.0 μV in ΔV_{BE} (for $\alpha = 16$), and a maximum relative error of about 0.0067% in α and 0.01% in m are found (for $\alpha = 16$, $T = 300$ K). The next step is to identify the accuracy-power tradeoffs in the interface circuitry, and then determine an appropriate level of power consumption.

C. Process Spread of V_{BE}

While ΔV_{BE} is insensitive to process spread, V_{BE} suffers strongly from process spread. Statistics about V_{BE} spread can be used to estimate the initial inaccuracy (without any correction) of V_{BE}, and so of the sensor. Typically, this spread results in errors of several degrees and so the sensor must be trimmed. The success of this approach, though, will depend on the identification and reduction of the main sources of V_{BE} spread, discussed as follows.

D. Spread Due to the Saturation Current I_S

The spread of the saturation current I_S of a PNP transistor is the main cause of V_{BE} spread. In order to see how this affects V_{BE}, a deviation ΔI_S from the nominal value I_S is introduced in the equation for V_{BE} given in (1), resulting in

$$\begin{aligned}
V_{\mathrm{BE}} &= \frac{kT}{q}\ln\left(\frac{I_{\mathrm{bias}}}{I_S + \Delta I_S}\right) \\
&\approx V_{\mathrm{BE}}|_{\Delta I_S = 0} - \frac{kT}{q}\frac{\Delta I_S}{I_S}, \quad (\Delta I_S \ll I_S).
\end{aligned} \tag{7}$$

This shows that the effect of the spread of I_{S} on V_{BE} is PTAT, if $\Delta I_{\mathrm{S}}/I_{\mathrm{S}}$ is assumed temperature independent. Thus, the spread of I_{S} causes the function $V_{\mathrm{BE}}(T)$ to rotate around a fixed point at 0 K. Because this PTAT error has only one degree of freedom, it can be trimmed based on a calibration at only one temperature, e.g. room temperature [7].

However, the assumption that $\Delta I_{\mathrm{S}}/I_{\mathrm{S}}$ is temperature independent is not necessarily true. Mechanical stress due to packaging may introduce a temperature-dependency to this ratio. Luckily, vertical PNP transistors are relatively insensitive to stress [7], which is why the temperature dependency of $\Delta I_{\mathrm{S}}/I_{\mathrm{S}}$ will be neglected in this work.

E. Spread Due to the Current Gain β

Because the PNP transistors are biased via their emitters, the collector current is given by

$$I_C = \frac{\beta}{1+\beta} I_{\text{bias}} \tag{8}$$

where β is the forward current gain. Substituting (8) in (1) results in

$$V_{\text{BE}} = \frac{kT}{q} \ln\left(\frac{\beta}{1+\beta}\frac{I_{\text{bias}}}{I_{\text{S}}}\right) \tag{9}$$

which reveals that V_{BE} depends also on β and, because of that, is sensitive to any process-spread on β. To see how this affects V_{BE}, a deviation $\Delta\beta$ from the nominal value β is introduced in (9), i.e.

$$\begin{aligned} V_{\text{BE}} &= \frac{kT}{q} \ln\left(\frac{\beta+\Delta\beta}{1+(\beta+\Delta\beta)}\frac{I_{\text{bias}}}{I_S}\right) \\ &\approx V_{\text{BE}}|_{\Delta\beta=0} - \frac{kT}{q}\frac{\Delta\beta}{\beta}\frac{1}{1+\beta}, \quad (\Delta\beta \ll \beta). \end{aligned} \tag{10}$$

This shows that V_{BE} is modified by an error term that is proportional not only to $\Delta\beta/\beta$, but also to the factor $1/(1+\beta)$. Because β is typically highly temperature dependent, the spread in β will cause a non-PTAT error in V_{BE}. This adds to the PTAT error due to the spread of I_{S}, resulting in an overall error with more than one degree of freedom. Depending on the magnitude of $\Delta\beta/\beta$, a single-temperature calibration may therefore be insufficient.

Equation (10) also shows that transistors with larger β are less sensitive to β spread. Unfortunately, vertical PNP transistors in CMOS technology tend to have a small β. In the 0.7 μm CMOS technology we used, β is approximately 22. If $\Delta\beta/\beta$ is assumed to be about 20%, a V_{BE} variation of about ± 0.25 mV results, which translates into a temperature error of about ± 0.1 °C. This shows that the effect of β spread in V_{BE} needs to be reduced if an inaccuracy of ± 0.1 °C is to be obtained using a single-temperature calibration. This need is even more acute in deeper sub-micron CMOS technology, where much lower values of β are found [5], [6]. A technique for making V_{BE} less sensitive to spread of β will be described in Section III-B.

F. Spread Due to Biasing Current

The bias current, I_{bias} in (9), also affects the accuracy of V_{BE}. Generally, this bias current is derived from a bias voltage using a bias resistor. As will be discussed in the following section, if a PTAT bias voltage is used, its contribution to process spread of I_{bias} can be made negligible. The bias resistor, however, will inevitably be subject to process spread. Provided the temperature dependency of this resistor is insensitive to process variations, the effect of this on V_{BE} is identical to that of the spread of I_{S}, i.e. it gives rise to a PTAT error in V_{BE}. Both errors can thus be corrected by a single PTAT trim.

III. Sensor Front-End

The sensor front-end, as shown in Fig. 2, is composed of a core that in effect generates V_{BE} and ΔV_{BE}, as described in Section II, and of a bias circuit that generates the PTAT biasing as needed in the core.

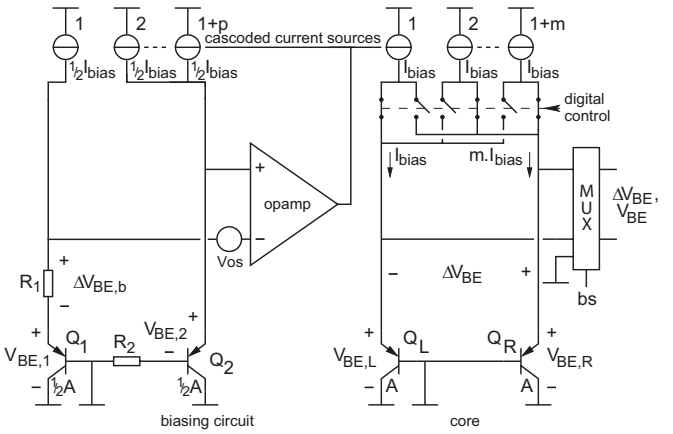

Fig. 2. Circuit diagram of the sensor front-end: biasing circuit and core (details of the bias-circuit chopping have been omitted).

In the core, Dynamic Element Matching (DEM) of current sources is used to provide an accurate current ratio m [9]. Every ΔV_{BE} cycle, a different unit current source is used to bias the transistor Q_{L} while the m remaining ones are used to bias Q_{R}. By alternating the unit current source, over $(1+m)$ ΔV_{BE} cycles, errors due to current-source mismatch are averaged out, so a more accurate 1:m ratio and thus ΔV_{BE} voltage is obtained [1]. The value of the ratio m and the bias current level, though, are subject to accuracy and power consumption constraints, as will be discussed below.

A. Current Ratio and Bias Current

When the PNP bias current is reduced so as to lower the front-end power consumption while keeping $(1+m)$ current sources for DEM, the approximation for V_{BE} as given in (1) is no longer accurate once the assumption of $I_{\text{C}}/I_{\text{S}} \gg 1$ no longer applies. In this case, V_{BE} is better approximated as (assuming for now $I_C = I_{\text{bias}}$)

$$V_{\text{BE}} \approx V_T \ln\left(\frac{I_{\text{bias}}}{I_S} + 1\right) \tag{11}$$

which results in a ΔV_{BE} given by

$$\Delta V_{\text{BE}} = V_T \ln\left(\frac{m I_{\text{bias}} + I_S}{I_{\text{bias}} + I_S}\right) \tag{12}$$

if the mismatch in the current sources and PNP transistors is negligible (i.e. $I_{\text{S,L}} = I_{\text{S,R}} = I_S$). The result in (12) shows that, regardless of how accurately m is established, the presence of the saturation current I_S will still cause a certain error in the value of ΔV_{BE}.

Though the magnitude of I_{S} can be reduced by reducing the emitter area of the PNP transistors, this is at the expense of poorer matching. The transistors also need to work in a region with neither low nor high injection effects and the region must have a constant current gain β [8].

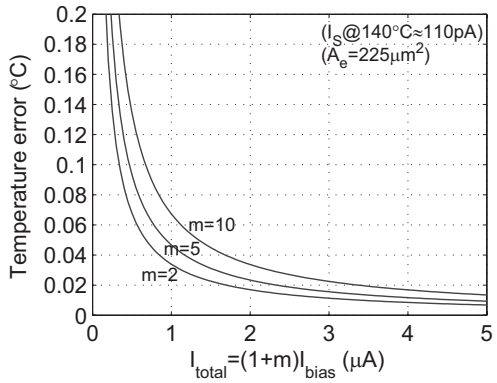

Fig. 3. Temperature error versus the total bias current I_{total}, for m = 2, 5, and 10. Results obtained for $I_{\text{S,max}} = 110$ pA (estimated for PNPs with emitter area $A_e = 225\ \mu\text{m}^2$ at $T = 140$ °C [10]).

The worst case relative error in the current ratio m is given by

$$\frac{\partial m}{m} = \frac{\frac{mI_{\text{bias}} + I_{S,\max}}{I_{\text{bias}} + I_{S,\max}} - \frac{mI_{\text{bias}}}{I_{\text{bias}}}}{\frac{mI_{\text{bias}}}{I_{\text{bias}}}} \tag{13}$$

where $I_{\text{S,max}}$ is the largest saturation current (i.e. at the highest temperature). According to (13), for a given m, a sufficiently high I_{bias} has to be chosen to keep the error below a given level.

However, it is more important to evaluate the error contribution due to the saturation current against the total bias current of the core, i.e., $I_{\text{total}} = (1 + m)I_{\text{bias}}$. Fig. 3 shows the simulated error contribution versus I_{total} for $m = 2$, 5 and 10. The results show that, for a given maximum error contribution, the required total bias current can be reduced by reducing the current ratio m. However, due to the resulting reduced sensitivity of ΔV_{BE}, this comes at the expense of more stringent offset and noise requirements on the A/D converter. As a compromise, m was set to 5. In addition, in order to limit the error contribution to below 0.02 °C, I_{bias} was set to 400 nA, giving a total bias current of about 2.3 μA. Because the bias current is PTAT, the value of 400 nA (at $T = 140$ °C) translates to a nominal bias current of approximately 250 nA at $T = 30$ °C.

B. PTAT biasing-Bias Circuit

A PTAT bias current [11] was chosen to bias the two PNPs Q_{L} and Q_{R} in the core. Compared to other types of bias currents, a PTAT current can be made relatively insensitive to process spread, as it is generated from a process-insensitive PTAT voltage. Thus, only the spread of the resistor R_1 (Fig. 2) causes significant spread of the currents [8]. Additionally, a PTAT current partially cancels the curvature of V_{BE} [12].

The bias circuit is built around a chopped opamp and two PNP transistors Q_1 and Q_2 biased at a 1:p current ratio (Fig. 2). Ignoring resistor R_2 for now, the opamp forces the PTAT difference $\Delta V_{\text{BE,b}}$ between the base-emitter voltages of these transistors to appear across resistor R_1, resulting in a PTAT unit bias current of $\Delta V_{\text{BE,b}}/R_1$.

Resistor R_2 has been added to implement a β-compensation scheme [1]. The voltage drop across R_2 due to the base current of Q_2 makes the bias current proportional to $(1 + \beta)/\beta$ for $R_2 = R_1/p$, so that it gives rise to a PTAT collector current when copied to the emitters of Q_{L} and Q_{R} in the core. Thus, errors in V_{BE} due to the spread of the PNP's finite current gain β are minimized.

As in the core, Q_1 and Q_2 are biased at a 1:5 current ratio ($p = 5$), but with a unit bias current of only 125 nA (half of that used in the core). Though a greater current ratio p would produce a greater $\Delta V_{\text{BE,b}}$, which is less sensitive to the opamp's offset, $p = 5$ is a better trade-off, reducing power dissipation at the expense of a small contribution to the sensor's inaccuracy (smaller than 0.03 °C).

Mismatch between the $(1 + p)$ current sources in the bias circuit gives rise to an error in $\Delta V_{\text{BE,b}}$, and hence in the PTAT bias current of the core. This, in turn, increases the spread of V_{BE} and thus the batch-calibrated inaccuracy of the sensor. Since the sensor is about an order-of-magnitude less sensitive to errors in V_{BE} than it is to errors in ΔV_{BE}, the matching requirement for the current sources in the bias circuit is much more relaxed than that for the current sources in the core. It can be shown that matching better than 0.15% is sufficient to reduce those errors to less than 0.01 °C. While DEM could be applied, a careful inter-digitated common-centroid layout was found to be sufficient to achieve this level of matching. The current sources of the core were included in this matched layout, to minimize the spread associated with current-source mismatch between the bias circuit and the core.

C. Trimming Approach

In order to correct for the process spread of V_{BE}, the same $(1 + m) = 6$ current sources of the core are used to digitally adjust the bias current of the PNP transistors when generating V_{BE} between I_{bias} and mI_{bias} (digital control in Fig. 2). Five of the six current sources are used to coarse trim the bias current. Because the sensor is designed to normally operate with two unit currents, there is one coarse step down and three up, which gives a near-balanced trimming capability due to the logarithmic dependency of V_{BE} on I_{bias}. To fine trim the sensor, the bitstream method [13] is used. The sixth current source is switched on and off, generating a bias current between 0 and I_{bias} depending on the output of a digital modulator. For a nominal bias current of 250 nA, an 8-bit modulator was used to obtain 1 nA trimming resolution.

IV. Incremental SC $\Delta\Sigma$ Analog-to-Digital Converter

The ratiometric measurement of $\alpha\Delta V_{\text{BE}}$ with respect to V_{REF} has been implemented using a second-order switched-capacitor (SC) incremental $\Delta\Sigma$ modulator. It is based on the design presented in [1], but differs from this design in two important aspects detailed below: a more power-efficient first integrator and a new temperature-dependent clocking scheme are employed.

A. Operating Principle

Fig. 4 shows a simplified circuit diagram of the modulator. It translates the output voltage of the front-end circuit $V_{\Delta\Sigma}$,

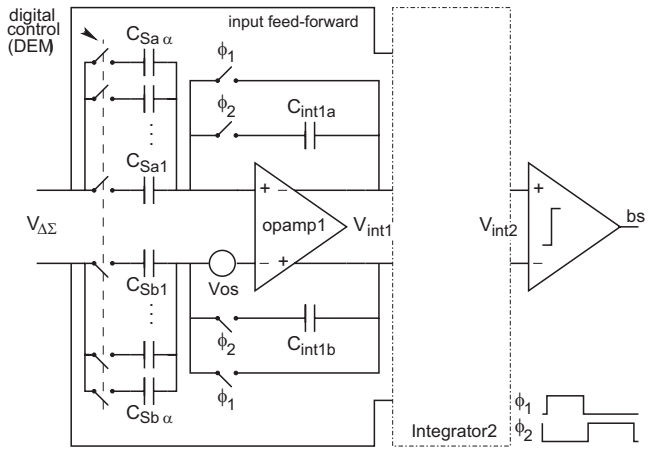

Fig. 4. Simplified circuit diagram of the second-order SC $\Delta\Sigma$ modulator.

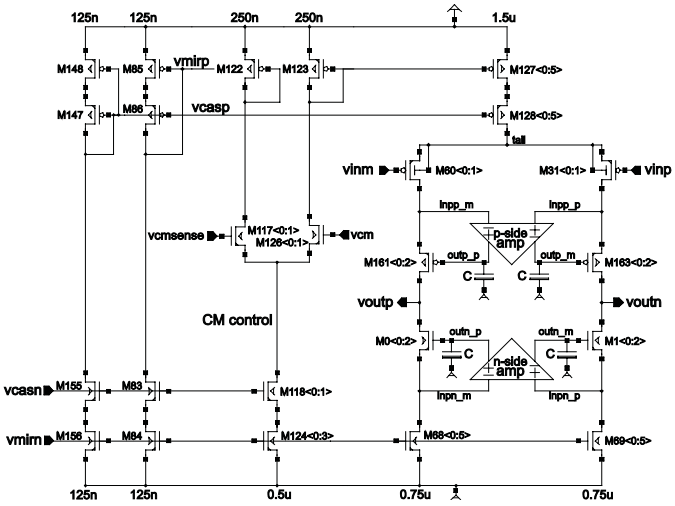

Fig. 5. Schematic of the fully-differential gain-boosted telescopic-cascode opamp used to implement the first integrator (implementation details of the gain-booster amplifiers have been omitted).

which is either $\Delta V_{\rm BE}$ (when $bs = 0$) or $-V_{\rm BE}$ (when $bs = 1$), into a bitstream bs whose average value μ equals the desired ratiometric function given by (4), as explained in Section II. A decimation filter (not shown), is used to decimate and scale this bitstream according to (5) to produce a digital output.

The modulator is operated using a two-phase non-overlapping clock. During phase ϕ_1, $V_{\Delta\Sigma}$ is sampled on capacitors $C_{\rm S}$, while during phase ϕ_2 the associated charge is transferred to the integration capacitors $C_{\rm int}$. When $bs = 0$ and $V_{\Delta\Sigma} = \Delta V_{\rm BE}$, all α capacitors $C_{\rm S}$ are used, whereas when $bs = 1$ and $V_{\Delta\Sigma} = -V_{\rm BE}$, only a single capacitor $C_{\rm S}$ is used. This implements the relative gain α as needed in (3). It is worth mentioning that the value of $\alpha = 16$ for $m = 5$ establishes a reference voltage $V_{\rm REF}$ that is slightly dependent on the temperature, which yields further compensation of the curvature of $V_{\rm BE}$ [12], in addition to the PTAT biasing. Because of the modulator's feedback, the average charge integrated over time is zero, i.e.

$$(1-\mu)\alpha C_S \Delta V_{\rm BE} + \mu C_S(-V_{\rm BE}) = 0 \qquad (14)$$

which results, when solved for μ, in the expression given by (4).

The size of the sampling capacitors ($C_{\rm S} = 2.5$ pF) was a trade-off between settling time, on one hand, and kT/C noise and most importantly charge injection error on the other.

To ensure that the modulator does not introduce any significant errors, several precision techniques are applied [1], [8]. Offset errors are reduced below 2 μV (which corresponds to 0.01 °C) by means of a combination of correlated double sampling (CDS) [14] in the first integrator and system-level chopping. Errors in the factor α due to capacitor mismatch are mitigated by applying dynamic element matching techniques, i.e. by dynamically interchanging the sampling capacitors $C_{\rm Si}$, $i = 1, 2, \ldots, \alpha$ (Fig. 4), so as to average out gain errors. Because the same integration capacitor $C_{\rm int}$ is used, regardless of the cycle, it does not affect α.

B. Modulator Implementation — First Integrator

The first integrator is built around a fully-differential gain-boosted telescopic-cascode opamp (shown in Fig. 5). Compared to the folded-cascode topology employed in earlier work [1], a notable power saving is achieved, since the telescopic topology only needs half the supply current of the folded version for the same transconductance and maximum output current. This comes at the expense of reduced output swing [15]. This can be accommodated thanks to the modulator's input feed-forward topology, which minimizes the output swing [1]. Since the integrator's CDS scheme requires unity-gain feedback, the opamp was designed to operate with identical input and output common-mode levels. Gain-boosting [16] was used to achieve a DC gain higher than a 100 dB over all process corners and operating conditions, so as to ensure negligible sampling errors. Nominally, the DC gain of the first integrator is 135 dB, with a GBW of 200 kHz. Including the boosting amplifiers, the opamp draws a total supply current of 4.5 μA.

C. PTAT Clock Frequency

Because of the PTAT biasing used in the front-end, the time needed for the modulator to settle is temperature dependent. Since the modulator's sampling capacitors (capacitors $C_{\rm S}$ in Fig. 4) are indeed the front-end's output load, charging these capacitors will take longer at low temperatures. This is shown in Fig. 6, where $V_{\Delta\Sigma}$ is the sampled voltage (either $V_{\rm BE}$ or $\alpha\Delta V_{\rm BE}$).

As a result, the use of a constant sampling clock frequency is sub-optimal in terms of settling time. A clock frequency optimized for accurate settling at high temperatures leads to errors at low temperatures due to incomplete settling. Conversely, a clock frequency optimized for accurate settling at low temperatures leads to a settling time that is over-designed, and hence less power-efficient, at high temperatures. Moreover, it will lead to increased errors due to leakage at the high end of the temperature range.

To accommodate accurate settling at both ends of the temperature range without these issues, the sensor uses a sampling clock with a temperature-dependent frequency. At low

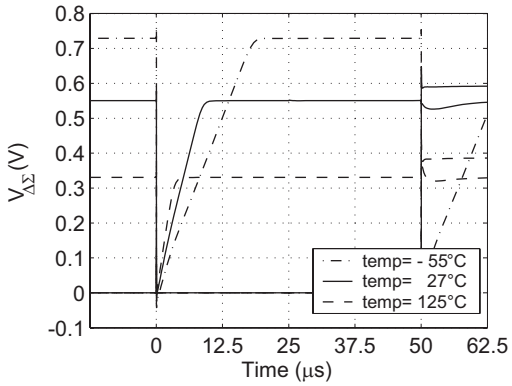

Fig. 6. Simulated slewing-time dependence on temperature (for a V_{BE} cycle, i.e., $V_{\Delta\Sigma} = V_{BE}$) for a fixed clock frequency $f = 10$ kHz.

TABLE I
SYSTEM (PTAT) CLOCK FREQUENCY

Temperature (°C)	From −50 to 130
Clock frequency (kHz)	8–17 (PTAT)

temperatures, the frequency is lower than its nominal value, allowing more time for settling, while at high temperatures, it is higher, reducing leakage errors by shortening the sampling period.

A nominal clock frequency of 11 kHz was chosen to ensure accurate settling at 30 °C. To find the optimal temperature dependency of the clock frequency, it is important to account for the fact that the settling consists of a slewing phase and an exponential settling phase [17]. Taking the temperature dependence of these phases into account, an optimal frequency of about 70% of the nomimal frequency is found at −55 °C, and about 140% of the nominal frequency at 125 °C. This leads to a frequency variation of about 1 kHz/20 °C, as shown in Table I. Because this temperature dependence is roughly proportional to absolute temperature, we refer to this as a PTAT clock frequency.

V. MEASUREMENT RESULTS

The temperature sensor was fabricated in a standard 0.7 μm CMOS process and encapsulated in a ceramic DIL package. A chip micrograph of the sensor is shown in Fig. 7. The die size is 4.5 mm^2, including bondpads. The chip contains all required circuitry, except for the clock generator and decimation filter of the $\Delta\Sigma$ ADC, which were implemented off chip for flexibility.

Measurements have been made on 20 samples from one batch. These samples were mounted, together with a precision platinum thermometer calibrated to 0.01 mK, on an aluminum block that provided thermal stability. This block, in turn, was placed in a climate chamber to vary temperature.

For all measurements presented below, the sensors were operated with a PTAT clock, as described in the previous section, and 1024 bits of their output bitstreams were decimated using a sinc^2 filter to calculate the bitstream average μ. This corresponds to a nominal conversion time of 100 ms. In this conversion time, the sensor achieves a resolution

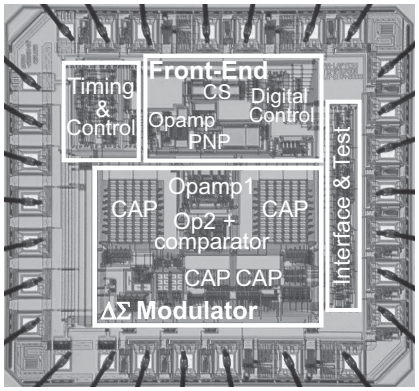

Fig. 7. Chip micrograph of the smart temperature sensor.

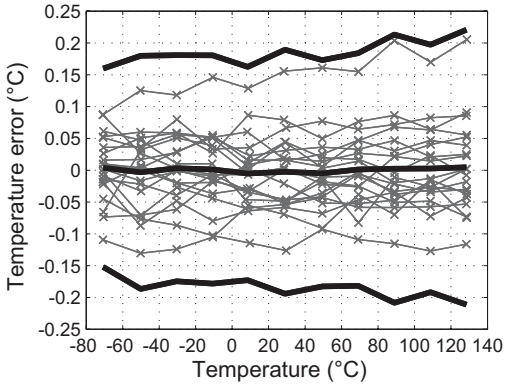

Fig. 8. Measured temperature error after batch calibration (20 samples with average and $\pm 3\sigma$ limits).

of 0.025 °C, which was measured by taking the standard deviation of successive readings at room temperature.

A. Batch-Calibrated Results

Four arbitrary sensors were initially characterized to perform the batch calibration. The bitstream average μ of each of these sensors was recorded over the operating temperature range. The coefficients A and B in (5) were then chosen such that the average measurement error of the four samples with respect to the platinum thermometer was minimized. The coefficients $A = 578.68$ and $B = -278.56$ thus found correct for the average offset and gain errors of the four samples, which is assumed to be a reasonable estimate of the average of the batch.

Fig. 8 shows the temperature error for all 20 samples when these same coefficients are used to translate their measured bitstream averages to temperature readings. To obtain these results, third-order curvature compensation was applied to remove the residual systematic non-linearity. This was less than 0.1 °C and was compensated for by adding a non-linear correction term, obtained from a look-up table, after decimation. At the high-end of the temperature range, the additive correction term also helps to reduce systematic errors due to leakage. Thus, an inaccuracy below ± 0.25 °C ($\pm 3\sigma$) was obtained from −70 to 130 °C, which is twice as good as the best batch-calibrated inaccuracy reported to date (refer to Table II). This level of accuracy is maintained for a

TABLE II
PERFORMANCE SUMMARY AND COMPARISON. ACCURACY FOM (ENERGY × ERROR × $\%^2$ IN nJ$\%^2$) LINE CALCULATED MOSTLY WITH DATA FROM [18]

Parameter	This Work	Pertijs [1]	Souri [6]	TMP275
Non-trimmed inaccuracy ($\pm 3\sigma$, batch calibrated)	±0.25 °C −70 °C to 130 °C	±0.5 °C −55 °C to 125 °C	±0.5 °C −30 °C to 125 °C	±1 °C max −40 °C to 125 °C
Trimmed inaccuracy ($\pm 3\sigma$, single trim at 30 °C)	±0.1 °C −55 °C to 125 °C	±0.1 °C −55 °C to 125 °C	±0.2 °C −30 °C to 125 °C	
Resolution	0.025 °C 10 conv./s	0.01 °C 10 conv./s	0.015 °C 10 conv./s	0.0625 °C 3.3 conv./s
Supply voltage	2.5–5.5 V	2.5–5.5 V	1.6–2 V	2.7–5.5 V
Supply sensitivity (at 30 °C)	0.05 °C/V	0.03 °C/V	0.1 °C/V	–
Front-end current	5 μA	37 μA	–	–
Supply current (cont. operation)	25 μA	75 μA	4.6 μA	50 μA
Accuracy FOM (nJ$\%^2$)	76	231	49	44 k
Technology	0.7 μm, CMOS	0.7 μm, CMOS	0.16 μm CMOS	–
Chip area	4.5 mm^2	4.5 mm^2	0.12 mm^2	–
Number of measured samples	20	24	19	–

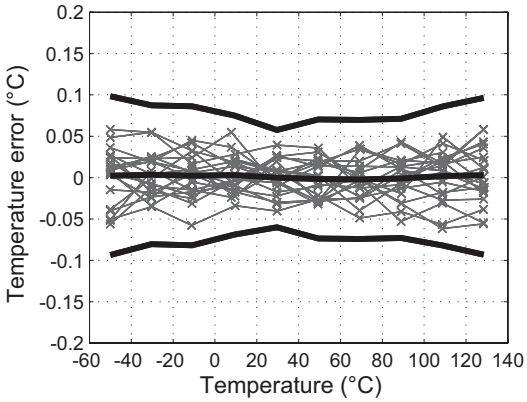

Fig. 9. Measured temperature error after trimming based on an individual calibration at 30 °C (20 samples with average and $\pm 3\sigma$ limits).

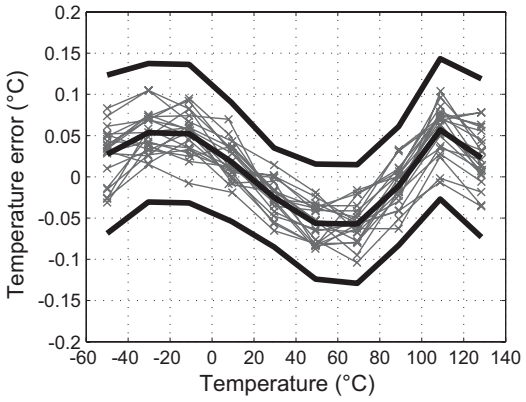

Fig. 10. Measured temperature error without compensation for systematic nonlinearity and leakage, after trimming based on an individual calibration at 30 °C (20 samples with average and $\pm 3\sigma$ limits).

supply-voltage range from 2.5 to 3.3 V, while the inaccuracy increases to ±0.3 °C for a supply voltage of 5.5 V.

B. Individually-Calibrated Results

Fig. 9 shows the temperature error after trimming based on an individual calibration at 30 °C. After correction for systematic non-linearity, a temperature error of ±0.1 °C ($\pm 3\sigma$) from −55 to 125 °C is achieved, which matches the state-of-art [1], but at 3 times less power consumption.

In addition, Fig. 10 presents the same result as that of Fig. 9, but without correction for systematic non-linearity. As expected, the inaccuracy of ±0.15 °C for the same temperature range is slightly worse, but it shows the well-defined and systematic curvature behavior of the samples, as well as a small systematic error due to leakage at 125 °C.

C. PTAT Clock Frequency Versus Fixed Clock Frequency

Measurement results comparing the sensor performance using the PTAT clock frequency (center frequency $f_{\mathrm{nom}} = 11$ kHz) and a fixed (11 kHz) clock frequency are shown in Fig. 11. As expected, the PTAT clock leads to the same performance as a fixed clock in the middle of the temperature range, but it delivers superior performance at the temperature extremes: up to 50% less batch-calibrated inaccuracy at −55 °C.

D. Measurement at 150 °C

The 20 samples were also tested up to 150 °C. At these temperatures, the PTAT clock frequency cannot compensate completely for the exponential rise in the leakage current. Therefore, clock frequencies higher than that defined by a PTAT characteristic were tested. The measured temperature errors, shown in Fig. 12, show a systematic non-linearity varying according to the clock frequency. For instance, at 150 °C, a systematic error (on average) of −0.9, −0.5, and 0 °C is observed for clock frequencies of 20, 25, and 35 kHz, respectively. Because of the very systematic error behavior, the same non-linearity correction used to handle the third-order

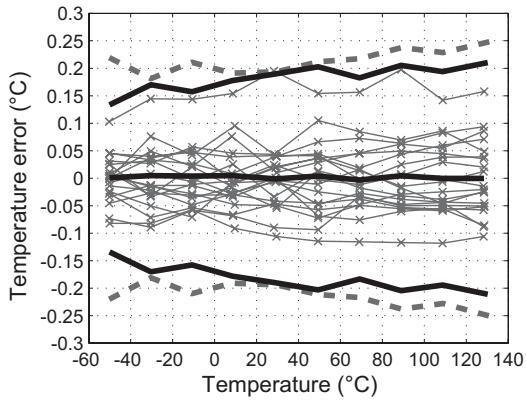

Fig. 11. Measured temperature error using a PTAT clock frequency (nominal frequency $f_{\text{nom}} = 11$ kHz) and fixed clock frequency ($f = 11$ kHz, dashed lines) (20 samples with average and $\pm 3\sigma$ limits).

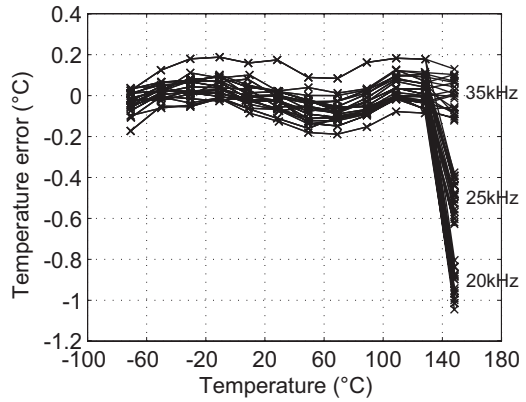

Fig. 12. Measured temperature error (extended range, up to 150 °C) after batch calibration, for three different clock frequencies at 150 °C: 20, 25, and 35 kHz (20 samples with no third-order curvature nor leakage correction).

curvature can be used to compensate for leakage at 150 °C. As shown, this extends the sensor's operating range up to 150 °C while maintaining ±0.25 °C inaccuracy.

E. Benchmark

Table II summarizes the measured performance of the 20 samples and compares it with other designs.

VI. Conclusion

This paper has presented the theory, design and implementation of a CMOS smart temperature sensor based on substrate PNP transistors and an incremental SC $\Delta\Sigma$ A/D converter. Without individual calibration, this sensor achieves an inaccuracy of ± 0.25 °C ($\pm 3\sigma$) from -70 to 130 °C, twice as good as that of the best ones reported up to now, while consuming only 62.5 μW during a measurement time of 100ms. This is accomplished by optimizing the power/inaccuracy tradeoffs and by incorporating several circuit techniques, discussed throughout the paper. After an individual calibration at room temperature, the sensor achieves an inaccuracy of ± 0.1 °C ($\pm 3\sigma$) over the military range, which matches the state-of-the-art, while consuming 3 times less energy per measurement.

References

[1] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ± 0.1 °C from −55 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, Dec. 2005.

[2] A. L. Aita, M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a batch-calibrated inaccuracy of ± 0.25 °C (3σ) from −70 °C to 130 °C," in *Proc. IEEE Int. Solid-State Circuits Conf.–Dig. Tech. Papers*, Feb. 2009, pp. 342–343.

[3] G. C. M. Meijer, "Concepts for bandgap references and voltage measurement systems," in *Advanced Analog Circuit Design*, Boston, MA, USA: Kluwer, 1996, pp. 243–268.

[4] M. A. P. Pertijs, A. L. Aita, K. A. A. Makinwa, and J. H. Huijsing, "Low-cost calibration techniques for smart temperature sensors," *IEEE Sensors J.*, vol. 10, no. 6, Jun. 2010, pp. 1098–1105.

[5] F. Sebastiano et al., "A 1.2V 10-μ W NPN-Based temperature sensor in 65-nm CMOS with an inaccuracy of 0.2 °C (3σ) from −70 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2591–2601, Dec. 2010.

[6] K. Souri and K. A. A. Makinwa, "A 0.12 mm 2 7.4μW micropower temperature sensor with an inaccuracy of ±0.2 °C (3σ) from −30 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 46, no. 17, pp. 1693–1700, Jul. 2011.

[7] G. C. M. Meijer, G. Wang, and F. Fruett, "Temperature sensors and voltage references implemented in CMOS technology," *IEEE Sensors J.*, vol. 1, no. 3, pp. 225–234, Oct. 2001.

[8] M. A. P. Pertijs and J. H. Huijsing, *Precision Temperature Sensors in CMOS Technology*. Dordrecht, The Netherlands: Springer-Verlag, 2006.

[9] G. C. M. Meijer, Patent Appl. 1 000 222, Apr., 1995.

[10] *Spice Models for C07MA and C07MD (CMOS 0.7 μm) - Under NDA*, AMI Semiconductor, Oudenaarde, Belgium, Jul. 2002, p. 21.

[11] G. C. M. Meijer, "Smart temperature sensor and temperature-sensor systems," in *Smart Sensor Syst.*, G. C. M. Meijer, Ed., New York, USA: Wiley, 2008, Ch. 7, pp. 185–223.

[12] G.C.M. Meijer, R. van Gelder, V. Noorder, J. van Drecht, and H. Kerkvliet, "A three-terminal integrated temperature transducer with microcomputer interfacing," *Sens. Actuators*, vol. 18, no. 6, pp. 195–206, Jun. 1989.

[13] M. A. P. Pertijs and J. H. Huijsing, "Bitstream trimming of a smart temperature sensor," in *Proc. IEEE Sensors*, Oct. 2004, pp. 904–907.

[14] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

[15] J. H. Huijsing, *Operational Amplifiers–Theory and Design*. Boston, MA, USA: Kluwer, 2001. pp. 261–269.

[16] K. Bult and G. J. G. M. Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB DC gain," *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1379–1384, Dec. 1990.

[17] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, Piscataway, NJ, USA: IEEE Press, 2005, pp. 283–297.

[18] K. A. A. Makinwa. (2012). *Temperature Sensor Performance Survey* [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor/survey.xls

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